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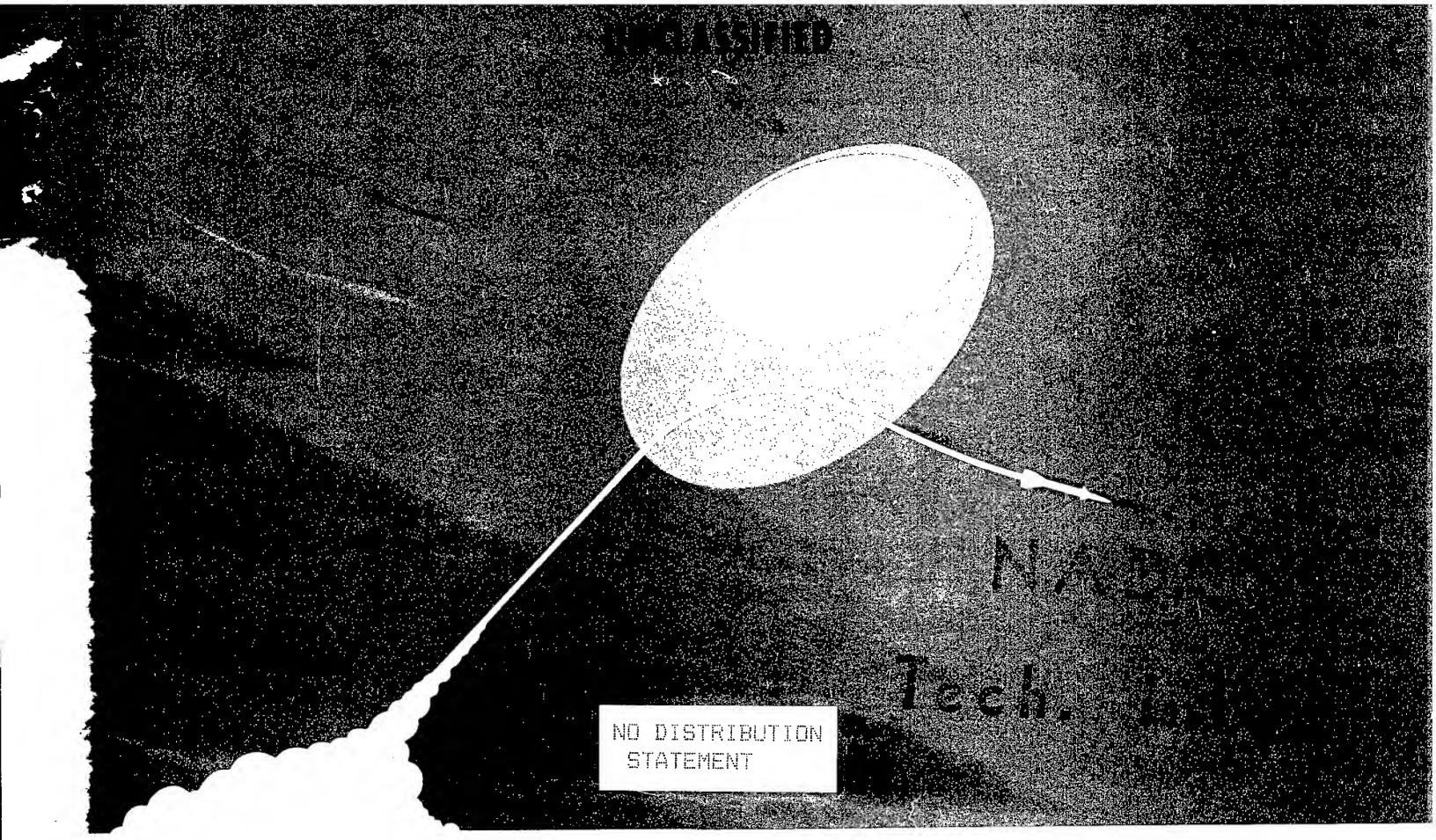

APPENDIX 18

TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION

FINAL SOFTWARE REPORT

DATA ITEM NO. A005

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INTEGRATED ELECTRONIC WARFARE SYSTEM
ADVANCED DEVELOPMENT MODEL (ADM)

78087-18

PREPARED FOR

NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PENNSYLVANIA

CONTRACT N62269-75-C-0070

RAYTHEON
ELECTROMAGNETIC
SYSTEMS DIVISION

1 OCTOBER 1977

UNCLASSIFIED

APPENDIX 18

TECHNIQUES GENERATOR SOFTWARE DESIGN SPECIFICATION

FINAL SOFTWARE REPORT

DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)
ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:

Naval Air Development Center
Warminister, Pennsylvania

Prepared by:

RAYTHEON COMPANY
Electromagnetic Systems Division
6380 Hollister Avenue
Goleta, California 93017

1 OCTOBER 1977

RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS. 02173	CODE IDENT NO. 49956	SPEC NO. 53959-HM-0412
			SHEET 1 OF / REV

TYPE OF SPEC

UNIT SOFTWARE DEVELOPMENT SPECIFICATION

TITLE OF SPEC

COMPUTER PROGRAM DESIGN SPECIFICATION FOR IEWS TECHNIQUES GENERATOR

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	H. McQuillen	8/5/76			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV
	9/13/76 Update Some Addresses In Flow Charts & Add List III.	A			

B

12/20/76

Changes are made in two modules, SC Technique-Channel Assignment, and SC Technique-Channel Parameter Change or Dismiss. The updated flow charts are:

Figure 7: Pg. 1-Added temporary storage (clear) for CFN.

Pg. 2-Added insertion of CHAN in word 9, and insertion of CFN in word 12.

Pg. 3-Added insertion of FN into CFN.

Pg. 4-Added restore of FM generator status when RR/RGPO Gen. unavailable.

Figure 8: Pg. 1-No change.

Pg. 2-No change.

Pg. 3-Added dismiss for RR/RGPO Gen., and for FM Gen.

Pg. 4-Added insertion of CHAN in word 9, and of FM Gen no. in word 12.

Table A gives address and data for eight Technique programs to be stored in the Techniques Program memory. These are selected samples used during TGU integration and test.

REVISION																								
SHEET NO.																								
REV STATUS OF SHEETS	REVISION																							
	SHEET NO.																							

IEWS SOFTWARE SPECIFICATION - COMPUTER PROGRAM DESIGN SPEC FOR TECHNIQUES GENERATOR

1.0 SCOPE

The computer program specified herein shall be entitled IEWS Techniques Generator Controller Program. The Techniques Generator Unit is part of the Integrated Electronics Warfare System, IEWS, being developed for test and evaluation to determine operational usefulness for advanced combat aircraft.

2.0 APPLICABLE DOCUMENTS

The following documents, form a part of this specification to the extent specified herein. In the event of conflict, the requirements of this specification shall govern.

AETD-XAV-1000	Experimental and Developmental Specification IEWS (Integrated Electronic Warfare System)
WS-8506	Requirements for Digital Computer Program Documentation

RAYTHEON SPECIFICATIONS

53959-HM-0410	Unit Hardware Development Specification - IEWS Hardware Spec. - Techniques Generator
53959-HM-0411	Unit Hardware Development Specification - IEWS Hardware Spec. - Transmitter Control - MAAS
53959-CD-1401	Interface Control Document Spec. - Daisy Chain Bus ICD
53959-JK-1003	Interface Control Document Spec. - Auxiliary Bus ICD

Eqpt. Division I — RP-16 Microprocessor

Eqpt. Division II — Computer Program Package Specification
Raytheon RP-16 Relocatable Macro
Assembler Functional Specification

3.0 REQUIREMENTS

3.1 FUNCTION/ALLOCATION DESCRIPTION

The IEWS Techniques Generator Controller Program shall be the software portion of Techniques Generator. It shall run in the T.G. Controller/Processor hardware which is implemented with an RP-16 Microprocessor. Together with the hardware, the program shall provide the overall T.G. functions described in paragraph 3.1.1, and the Controller/Processor functions described in paragraph 3.1.2.1, both of applicable document 53959-HM-0410, T.G. hardware specifications.

The TG Controller Program shall be structured in the modules and relationships as shown in Figure 1. Bascially, once initilized, the program shall be interrupt-driven. The two hierarchy modules are Initilize (INLZ), and Loop (LOOP). At power up or as required, the System Controller, SC, or a Local Control Panel, LCP, shall be able to put the program to start of INLZ. Either of the two shall be able to command run.

INLZ shall initilize all variables, assignments and generators and transfer to LOOP. LOOP shall bascially enable interrupts and run in an idle loop awaiting interrupts. All service routines shall return to LOOP to await further interrupts.

There shall be twelve types of interrupt service modules as shown in Figure 1 and Figure 2, VIZ.,

SC Write Fault (SCWF)
SC Assignment - Frequency, ACN (SCAFA)

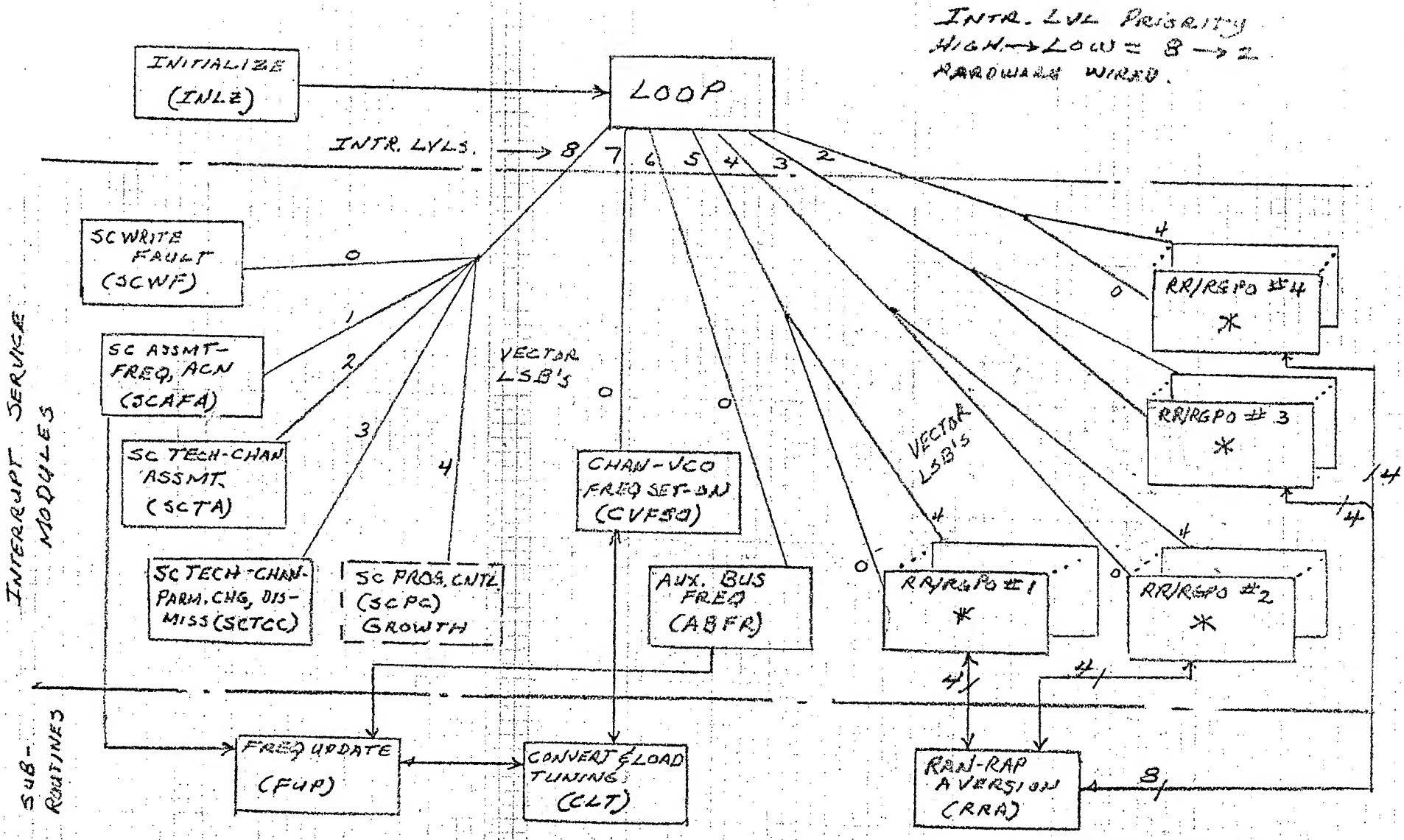


FIG. 1. TECH GEN. UNIT-CONTROLLER SOFTWARE

PAGE 1 of 2

W. McLuckie 7/22/76

See Fig. 1 for
MODULE RELATIONSHIPS
TO REMAINDER OF
PROGRAM

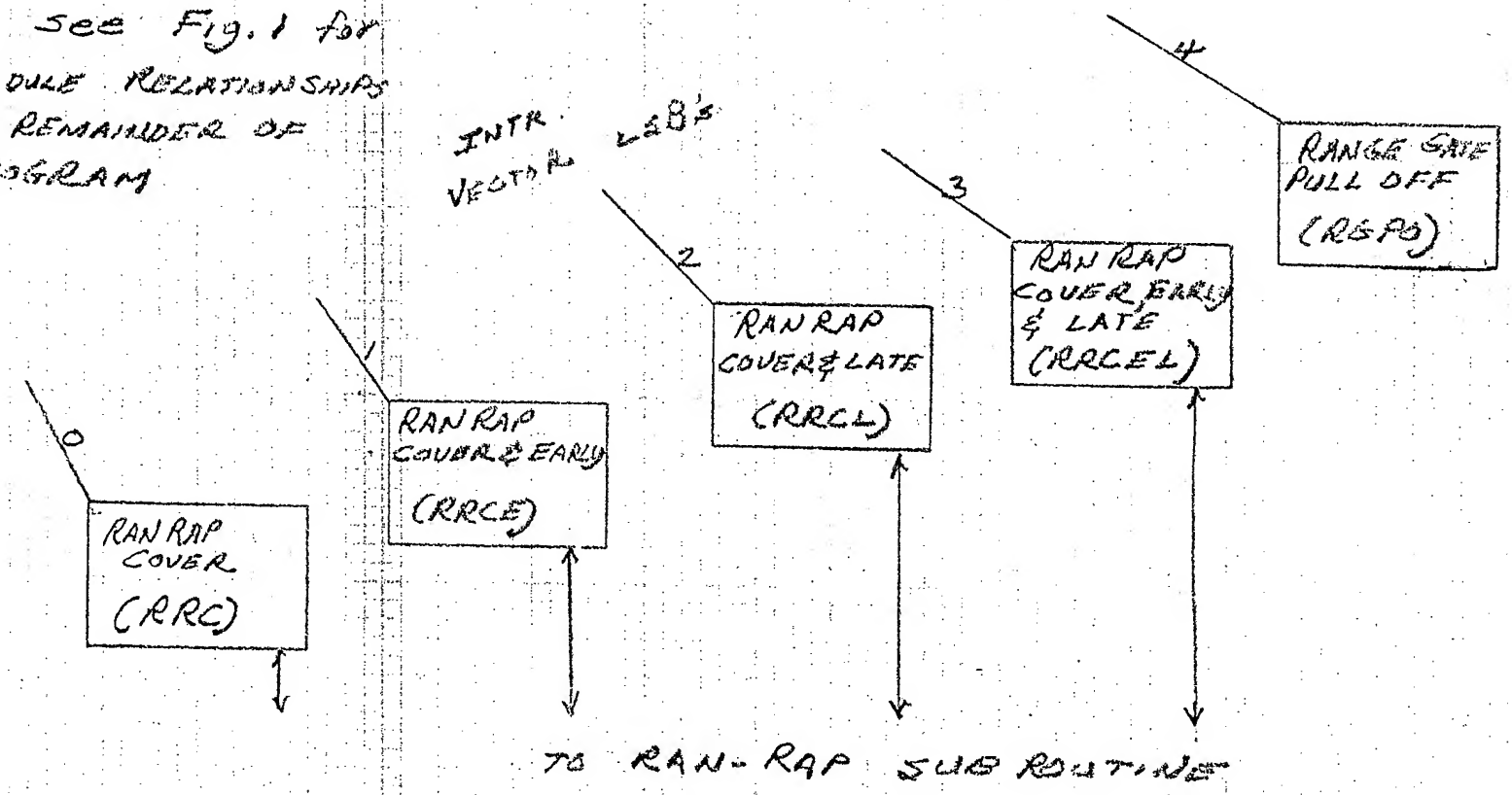


FIG. 2 RR/RGPO MODULE TYPES

H. McAllister
7/22/76

SC Technique-Channel Assignment (SCTA)

SC Technique-Channel Parameter Change, Dismiss (SCTCC)

SC Program Control (Currently Growth) (SCPC)

Channel-VCO Frequency Set-On (CVFSO)

Auxiliary Bus-Frequency (ABFR)

RAN-RAP Cover (RRC)

RAN-RAP Cover and Early (RRCE)

RAN-RAP Cover and Late (RRCL)

RAN-RAP Cover, Early, Late (RRCEL)

Range Gate Pull-Off (RGPO

Note in Figure 1 that the last five module types shall service four RAN-RAP RGPO Technique Generators. Interrupt level selects the general service. Within the interrupt level the three least significant bits, LSB's, of the hardware interrupt vector shall identify a particular service module. Within any of these levels, the device requesting service determines the vector, only one vector per service request.

Interrupt services have horizontal modularity, i.e., service routines are independent of one another.

Finally, there are three subroutines:

Frequency Update (FUP)

Convert and Load Tuning (CLT)

RAN RAP -A Version (RRA)

Relationships of subroutines to service module users are shown in Figures 1 and 2.

At the end of any service-routine execution, the program shall return to LOOP. For this development the software shall enable interrupts only during LOOP. Nesting of interrupt services is a software growth capability. The hardware is capable of supporting such nesting.

3.2 FUNCTIONAL DESCRIPTIONS

Each IEWS T.G. Controller Program module shall implement the corresponding flow diagram given herein. Each flow diagram shows the fixed hardware addresses involved. Externally interchanged word formats shall be as specified in the referenced, associated document, 53959-HM-0410, "Unit Hardware Development Specification - IEWS Hardware Spec. - Techniques Generator". Programmable variables within programs shall have the values given on the diagrams. Some of these modules might change as a result of development tests. Internal word formats can vary from those herein if more practical. Program Tables are given in paragraph 3.3

3.2.1 Initialize (INLZ) Module

INLZ shall be as given in Figure 3. Controls and address to set and run INLZ are given in notes thereon. INLZ clears all assignments, if any, and flags. It initializes all internal tables.

3.2.2 Loop (LOOP) Module

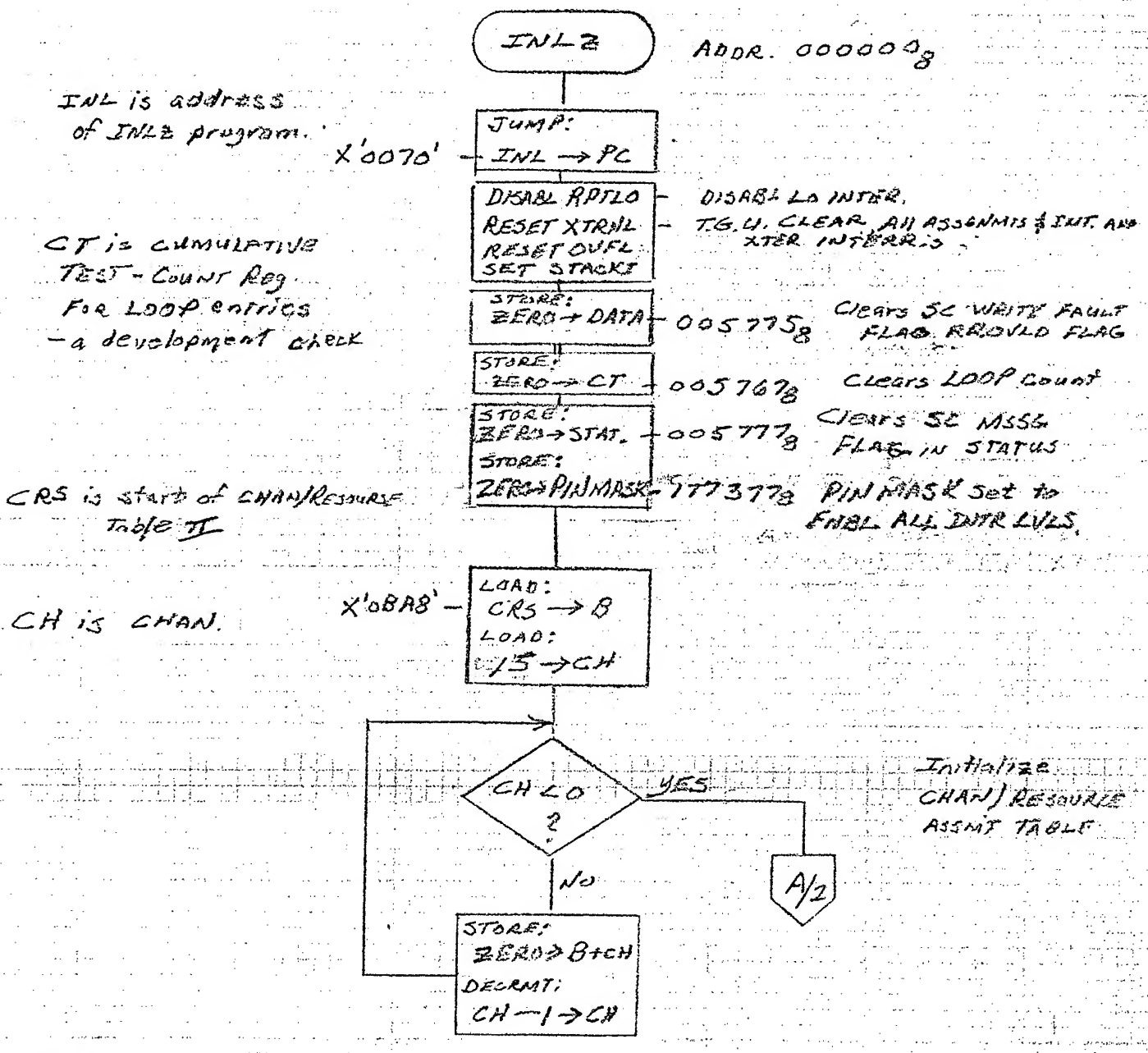
LOOP shall be as given in Figure 4. Background testing can be added to this at any time as growth software.

3.2.3 SC Write Fault (SCWF) Module

SCWF shall be the interrupt routine of Figure 5. Hardware interrupt vectors and addresses are given. This routine endeavors notify the SC if a write is attempted to T.G. instruction memory during times of memory-protect. The T.G. RP-16 4K word memory is two-port, one for the Daisy Chain (DC) bus, and the other for the T.G. RP-16. The memory is

FIG. 3 INITIALIZE

PAGE 1 of 3



NOTES: 1. INITIALIZE address 0000_H is set for any:

a. SC Daisey Chain Master Clear - DCMCL
b. LCP Master Clear - MSTCL
c. SC TG External Control "Initialize"
d. LCP Control "STOP" and by inputting Addr. 0000_H.

2. Subsequent Jumps to INITIALIZE RUN either:

a. SC TG External Control "NEW START"
b. LCP Control "START" (at Addr. 0000_H)

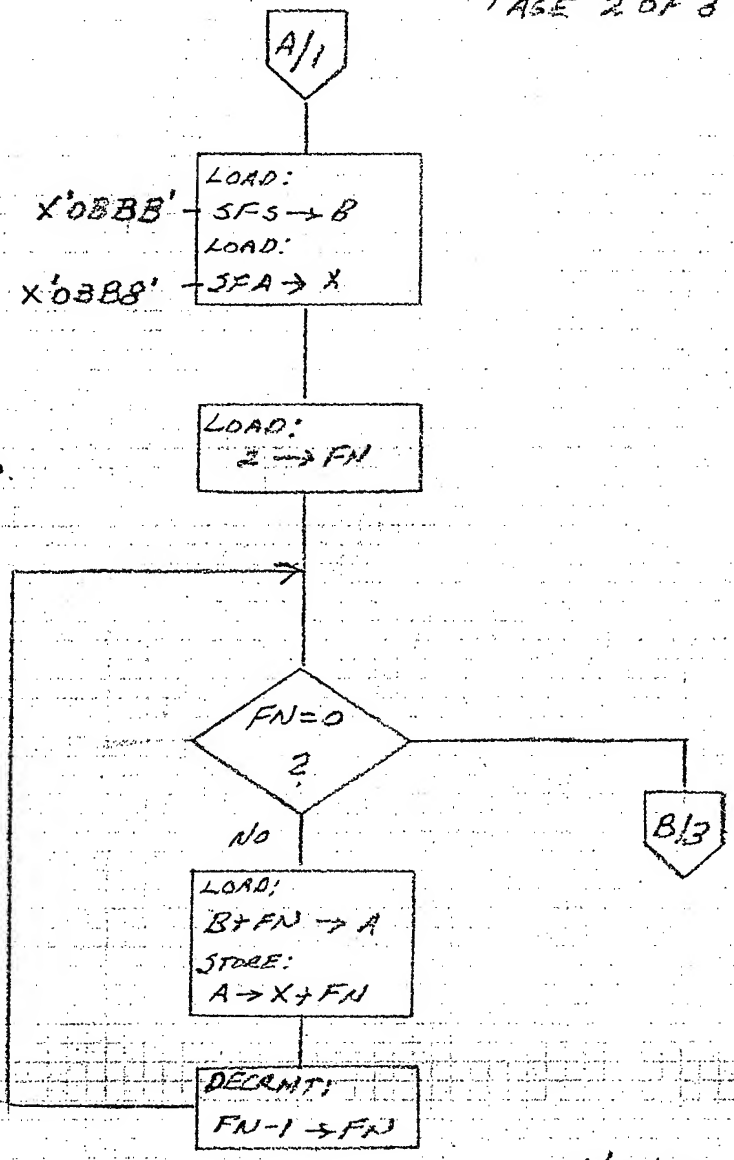
H. McCandless
7/28/76

FIG. 3 (CONT'D) INITIALIZE
ADDED 11/27/74

SFS IS START OF FM GEN PRE-OPER. STATUS TABLE IN A

SFA IS START OF FM GEN ALLOCATION (OPER.) TABLE IN A

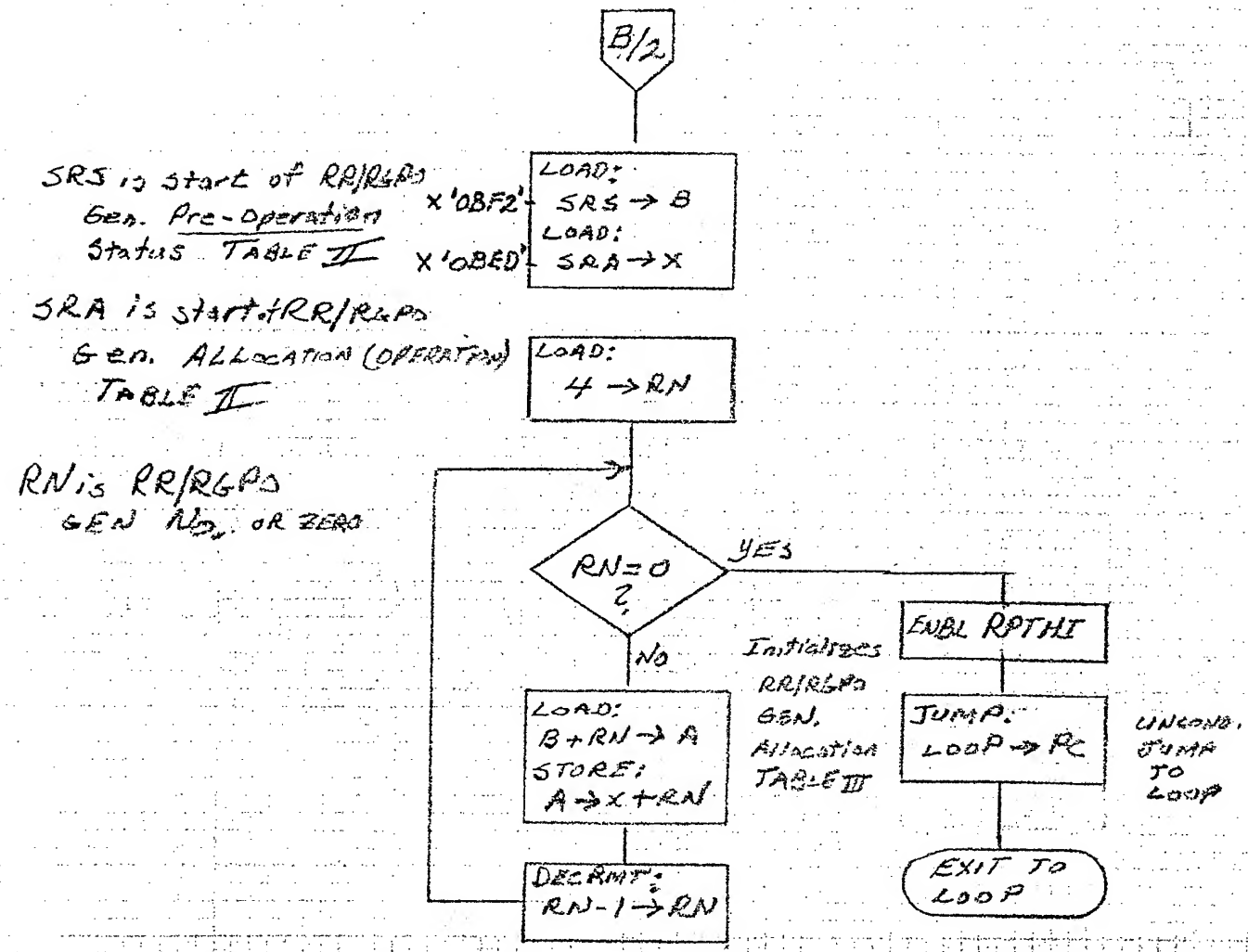
FN IS FM GEN NO.



11/29/74
Howard McDuffie

FIG. 3 (CONT'D) INITIALIZE

PAGE 3 OF 3

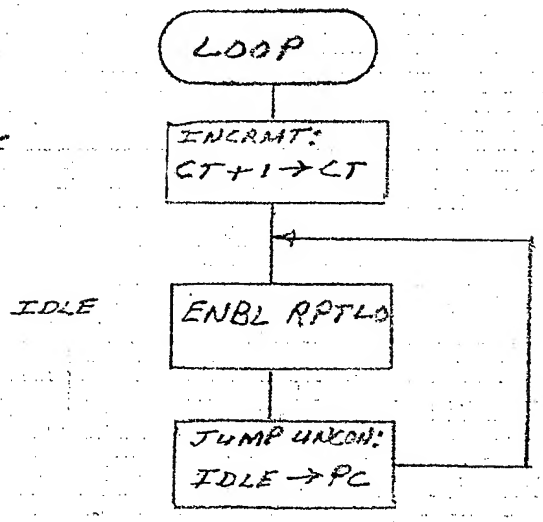


7/29/76

H. McLaughlin

FIG. 4 LOOP

CT is cumulative Test

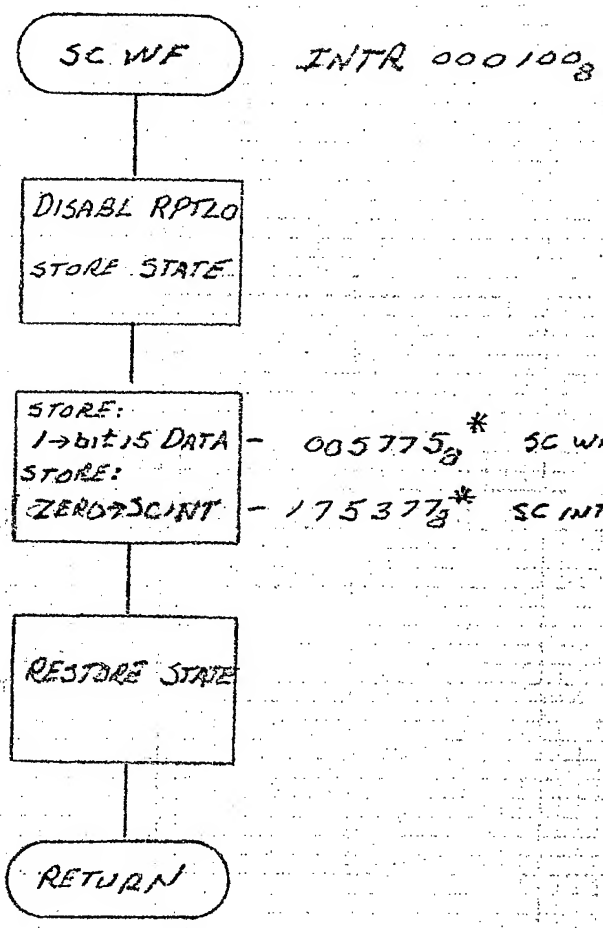


NOTES: 1. LOOP is ENTERED WITH JUMP from:
a. INITIALIZ (INLZ),
b. Return from any other INTERRUPT ROUTINE MODULE

2. Cumulative Test is Count of LOOP entries subsequent to INLZ. This is a check during Devlpmt Tests

H. McAuliffe 7/28/76

FIG. 5 SC WRITE FAULT



*NOTE:

1. 175377_8 Addr. Sets SC INTR(8) on the Daisy CHAIN B:15. The Bus has no INTR ACK. Hence -
2. The INTR RQS (8) remains set until:
   a) SC addresses 005775_8, or
   b) SC issues DC MCL, or
   c) If programmed, TG RP-14 "RESET XTRNL", i.e. OPRST.

7/26/70 - R. The Faulkner

partitioned with T.G. instructions, data, and working space in all but 8 locations. It is the bulk of this memory except the 8 locations for SC messages that is at times protected to DC writes. An SC Daisy Chain Master Clear, DCMCL always opens all memory to DC write. Any time a message is transferred through any of the 8 message locations the bulk of memory is protected from DC writes. If while protected a DC write is attempted, DC ACKnowledge is hardware returned to prevent hanging the bus, even though data is not written. The T.G. RP-16 receives the interrupt and in turn attempts to notify the SC as shown in Figure 5. The 4K memory is open to DC read all the time. The two port is used to facilitate loading T.G. RP-16 program directly from the DC bus.

3.2.4 SC Assignment-Frequency, ACN (SCAFA)

SCAFA shall be the interrupt routine of Figure 6. Note that the Frequency Update Subroutine (FUP) is used in this service. Return to LOOP is from FUP.

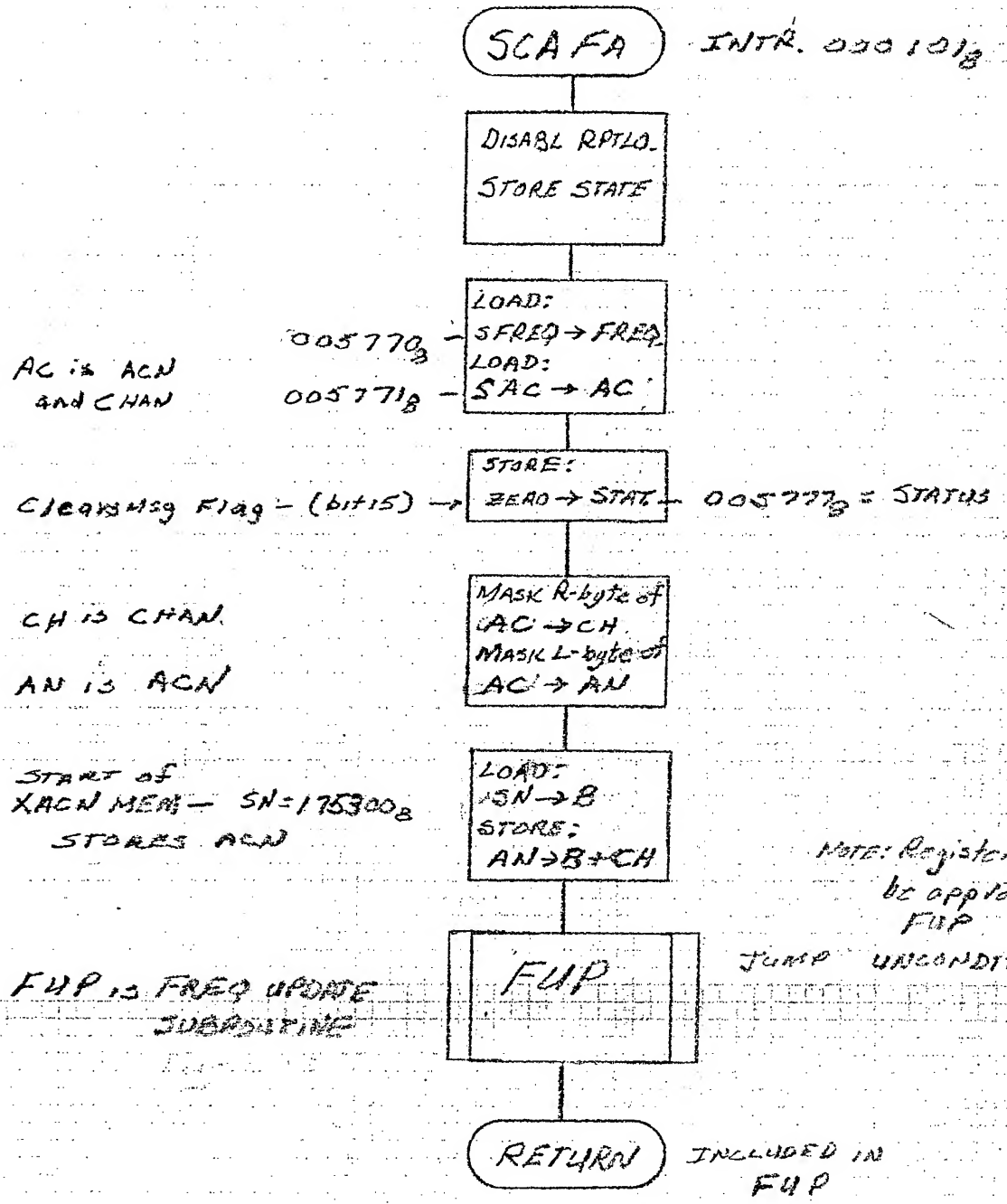
3.2.5 SC Technique-Channel Assignment (SCTA) Module

SCTA shall be the interrupt routines of Figure 7. This module retrieves all generator parameters from T.G. Techniques Program memory and loads the proper generators. Where the limited number of RAN-RAP/RGPO generators are needed, the routine performs a resource management allocation by finding an unused generator for the current program. It remembers to which channel the generator is assigned.

3.2.6 SC Technique-Channel Parameter Change or Dismiss (SCTCC) Module

SCTCC shall be the interrupt routines of Figure 8. This module changes any parameters of a currently assigned Technique Program per the SC message. The Technique Program stored in Technique Program memory remains as originally loaded. If the change is in use of the Auxiliary Bus for Frequency and/or ACN, the routine fills in the balance of the word as stored in Techniques

Fig. 6 SC ASSIGNMENT - FREQ, ACN



7/26/76
H.R. McQuillan

FIG. 7 SC TECHNIQUE - CHANNEL ASSIGNMENT

REDONE 11/30/72 REVISED 12/10/72

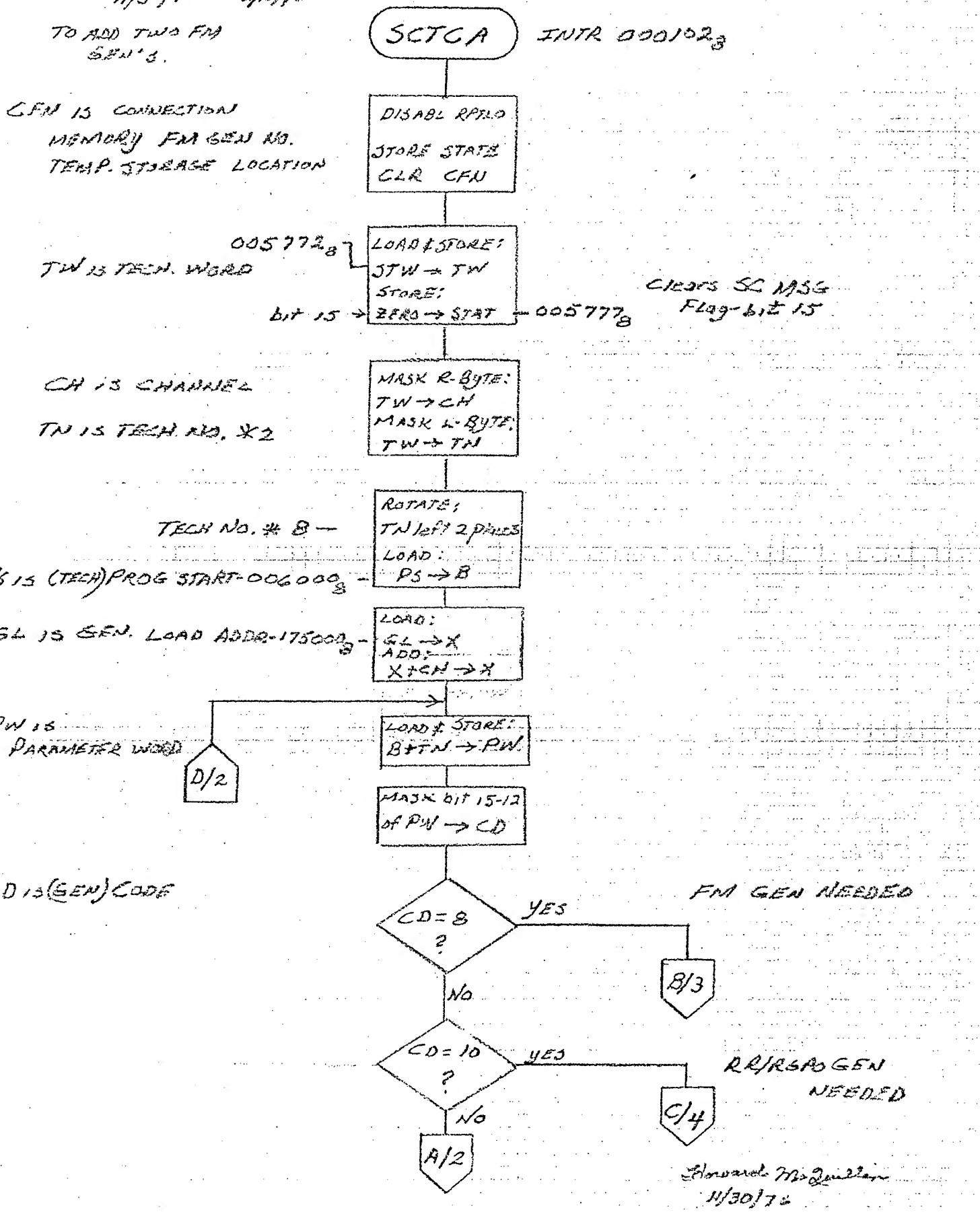
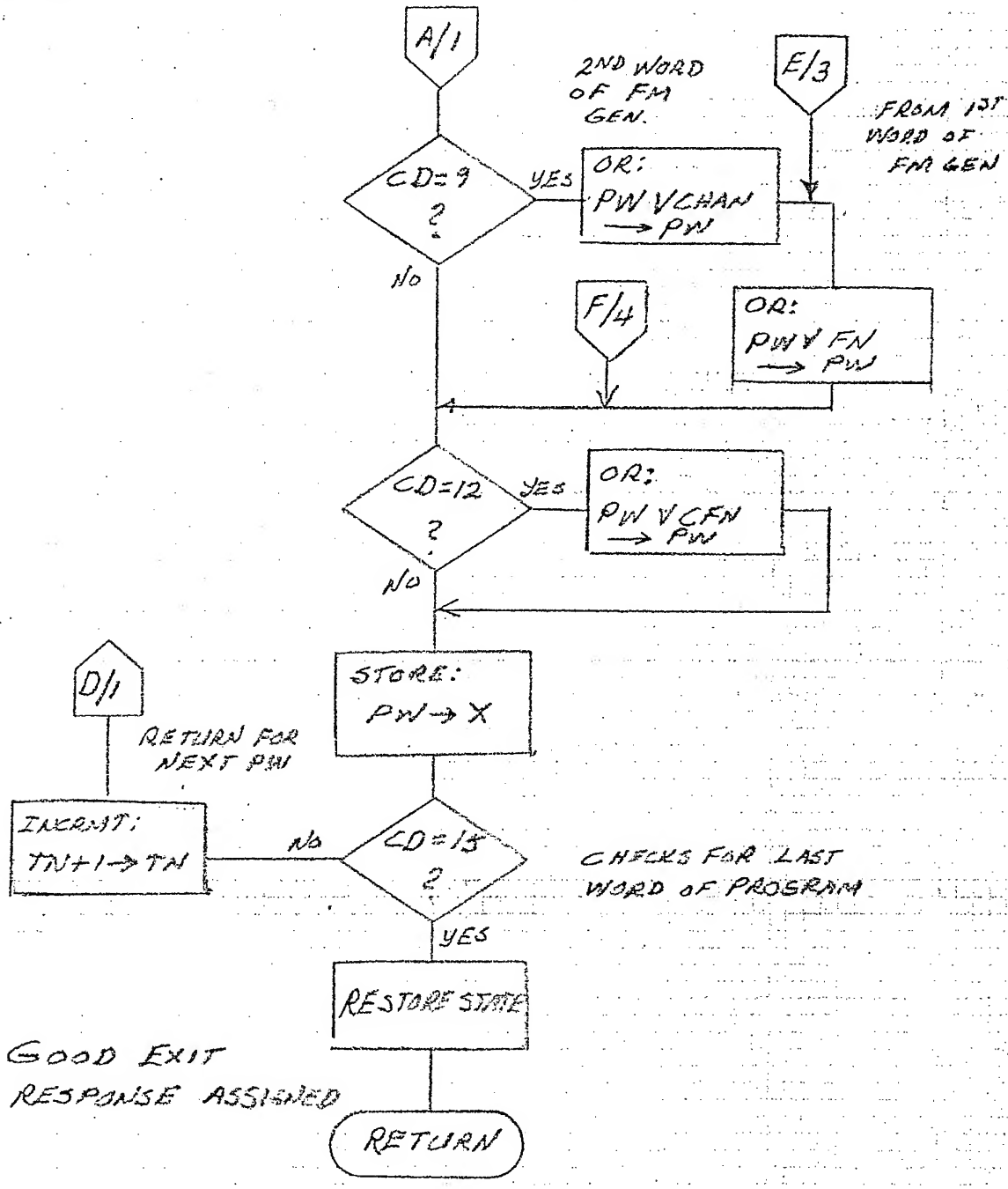


FIG. 7 SC TECH-CHAN ASSMT (CONT'D)

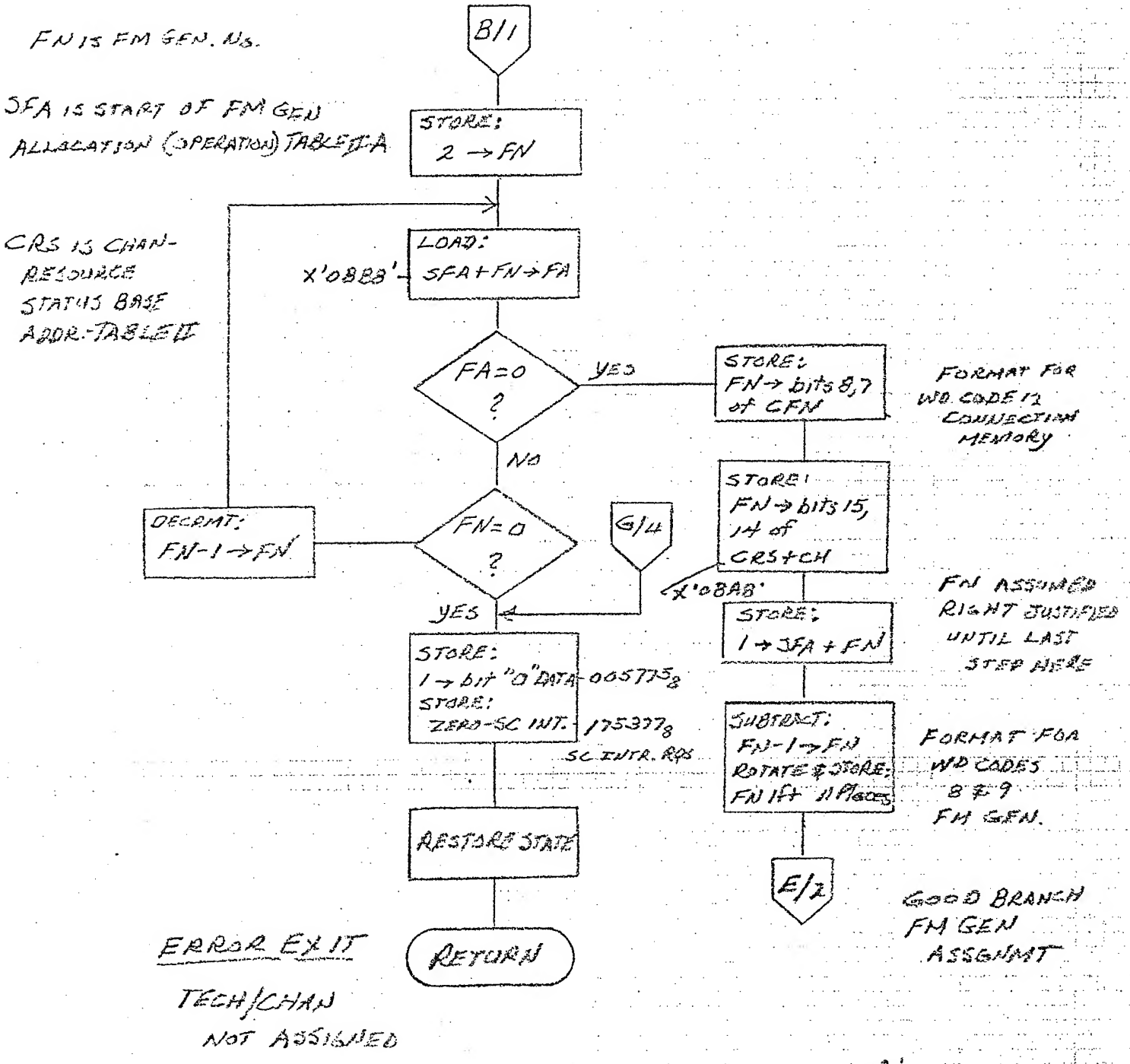
REDONE 12/10/76



Howard R. Gullin
12/10/76

FIG. 7 SC TECHNIQUE - CHANNEL ASSGT (CONT'D)

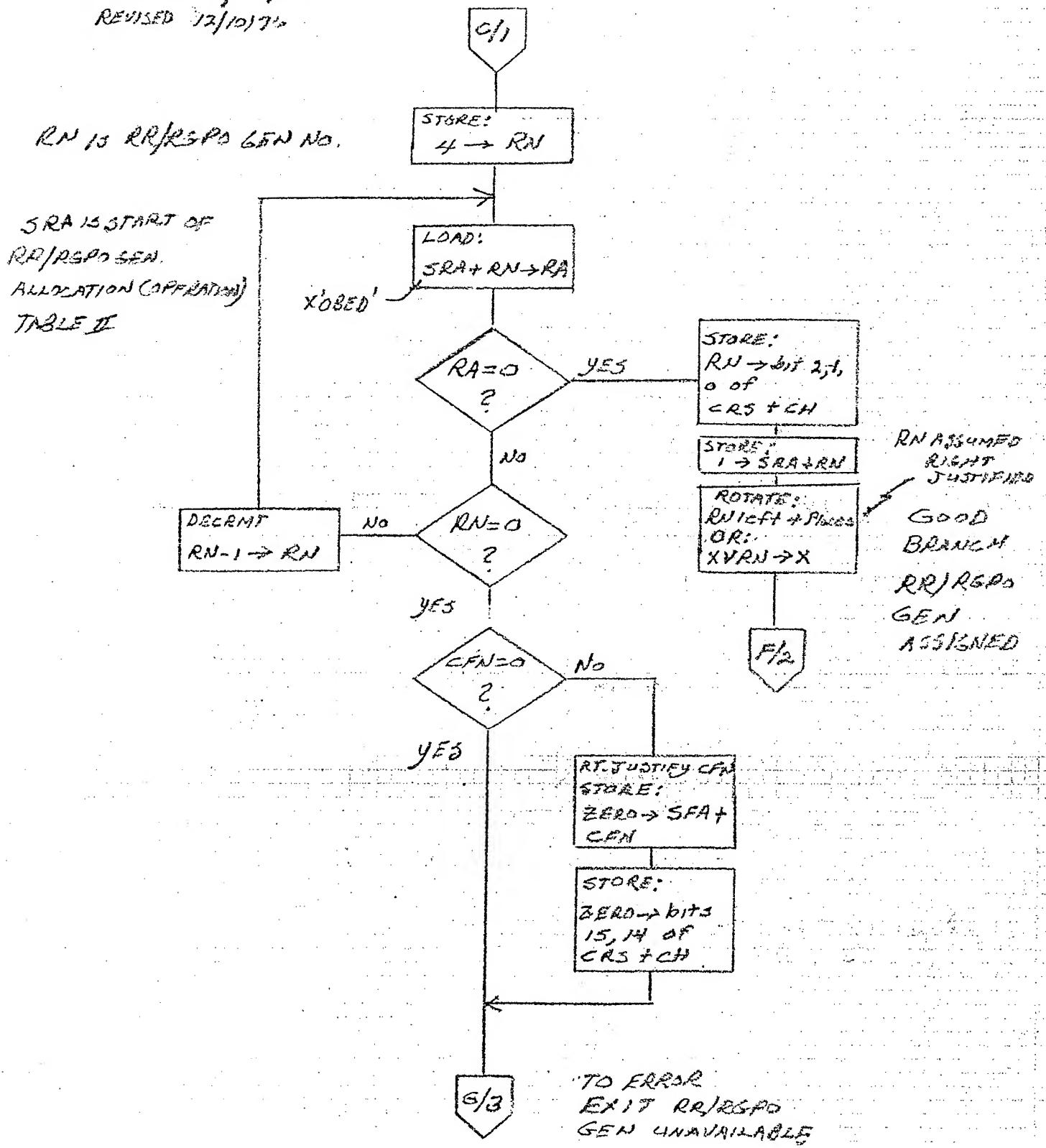
REDONE 11/30/76
REDONE 12/10/76



Howard McDuffie
12/10/76

FIG. 7 SC TRAN-CHAN ASSMT (CONT'D)

REDONE 11/30/76
REVISED 12/10/76



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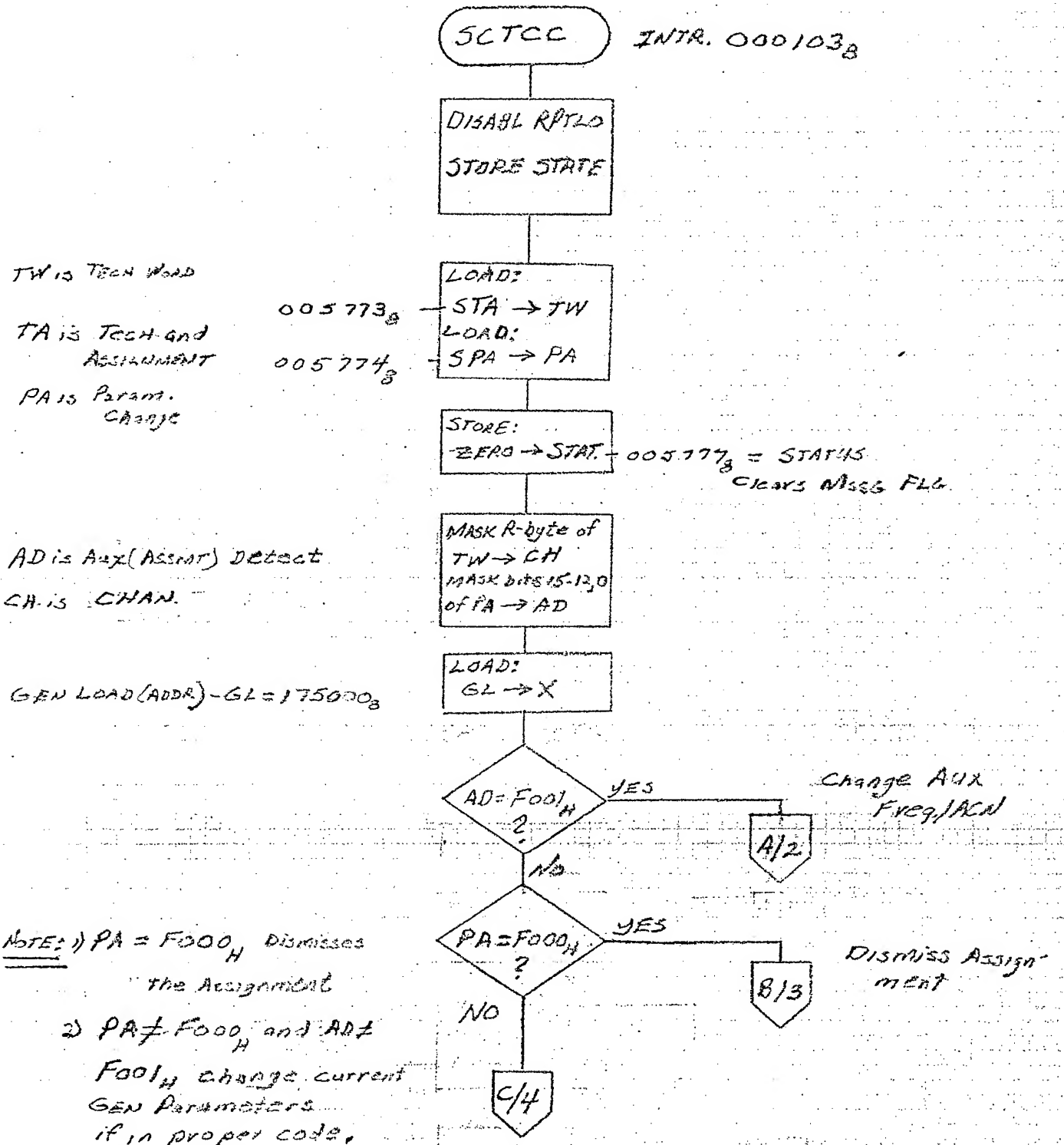
11/30/76
12/10/76

Fig. 8 SC TECHNIQUE - CHANNEL PARAMETER CHANGE OR DISMISS

PAGE 1 of 4



NOTE: 1) PA = F000H Dismisses the Assignment

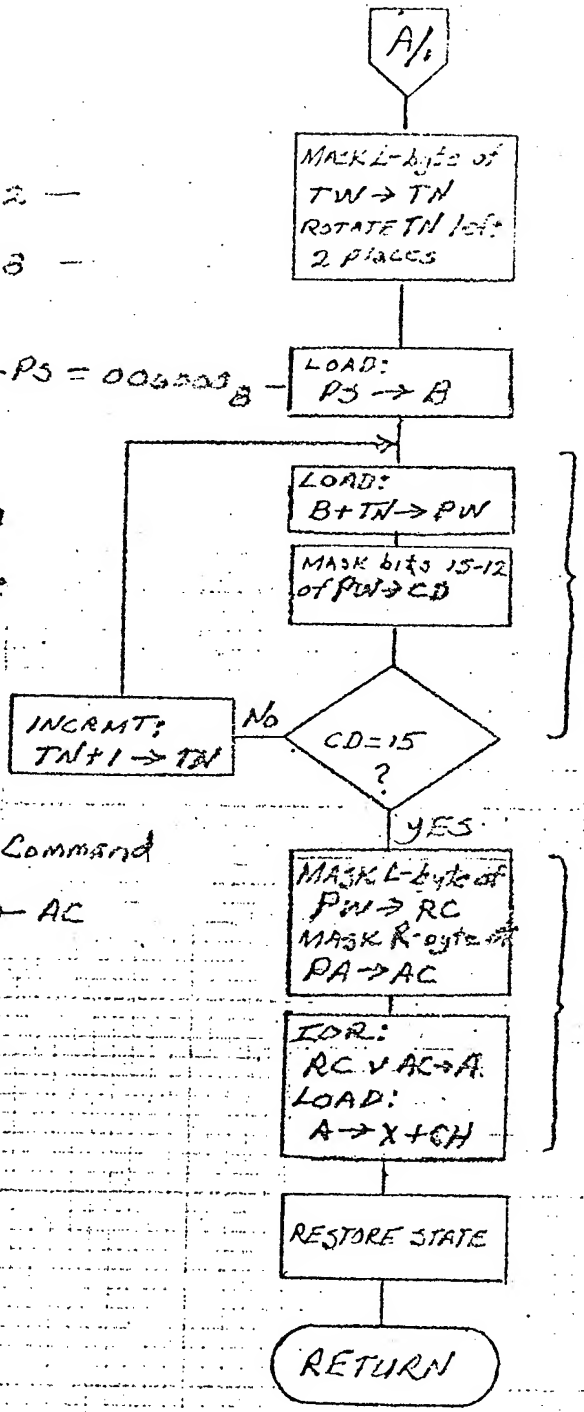
2) PA ≠ F000H and AD ≠ F001H change current GEN Parameters if in proper code, PA does not change parameters in Tech Prog. Memory

3) See format of PARAM. WORD: GEN CODE FH

4) DCMCL or other control (Fig. 3) To INIZ dismisses all channel assignments.

R. McClellan
7/23/76

Fig. 3
SCTTC (Cont'd) PAGE 2 of 4



TN is Tech. No. * 2 —

TN is Tech. No. * 3 —

(TECH) PROG START – PS = 000200 $_8$ –

PW is Param. Word

CD is (GCA) Code

RC is Response Command

AUX (Bus) Command — AC

This routine changes AUX B IS ASSMT – ACN OR FREQ FOR THIS CHANNEL PER SC COMMAND

Fetch Techn. Memory END word.

Combine Techn. Memory XPDR, RPTR, & CW bits of END word with new AUX Bus assignment of PA

H R McQuillen
7/23/76

FIG. 8 SC TECH-CHAN PARAM. CHG OR DISMISS JCT<< (CONT'D)

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REVISED 12/10/76

THIS ROUTINE DISMISSES A CHAN ASSMT INCLUDING RESOURCES REQ'D AND/OR FM GEN IF ASSIGNED

CRS IS CHAN-RESOURCE STATUS ADDR BASE TABLE II

RN IS RQ/RSPD GEN NO. ASSIGNED TO THIS CHAN

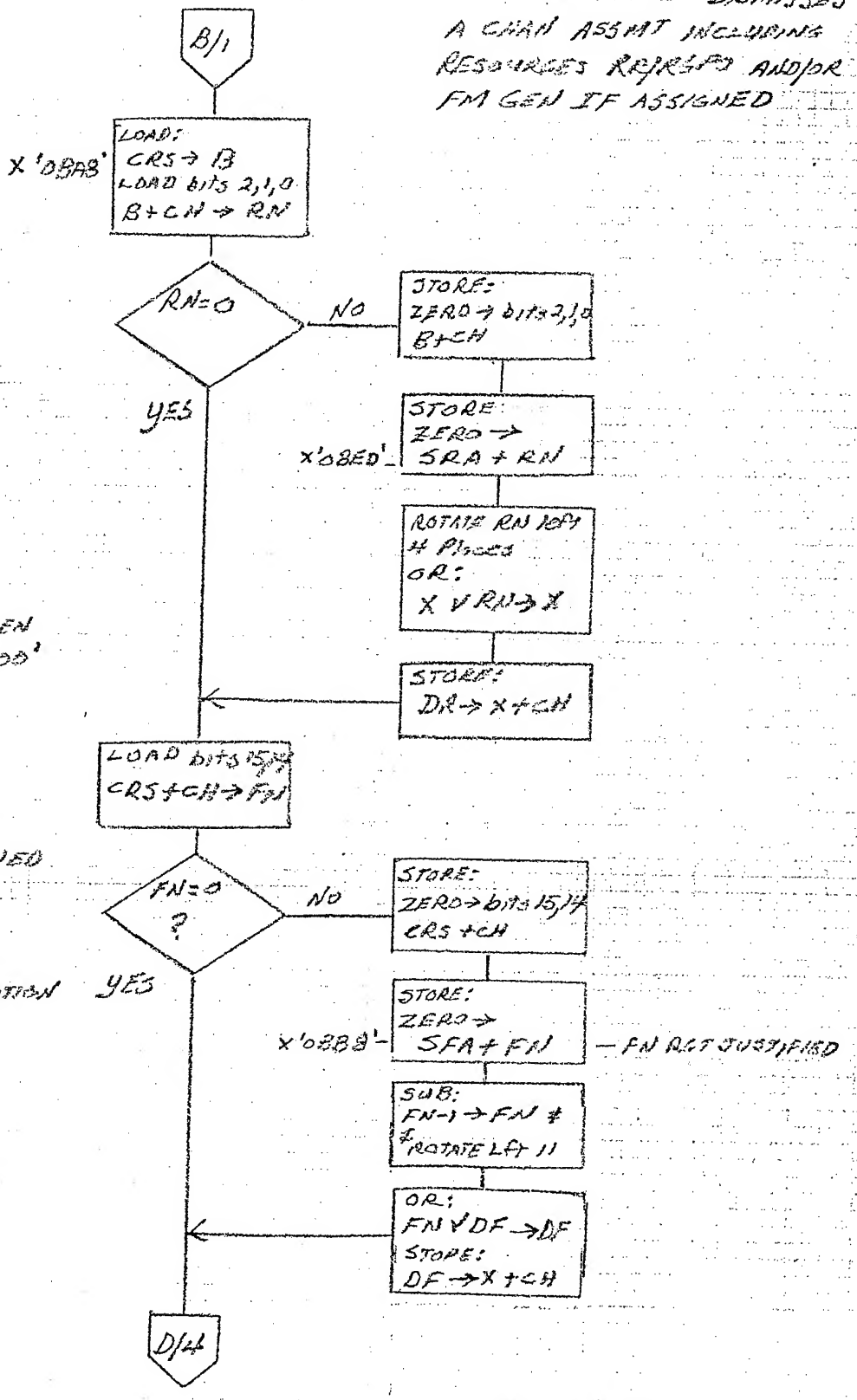
SRA IS RQ/RSPD GEN ALLOCATION TABLE II

DR IS DISMISS RQ/RSPD GEN AND EQUALS X'8000'

FN IS FM GEN NO. ASSIGNED TO THIS CHANNEL

SFA IS FM GEN ALLOCATION TABLE II A

DF IS DISMISS FM GEN AND EQUAS X'8000'



Howard McQuillen
12/10/76

FIG. 8 SC TECH-CHAN PARAM. CHG OR DISMISS SCTLC (CONT'D)

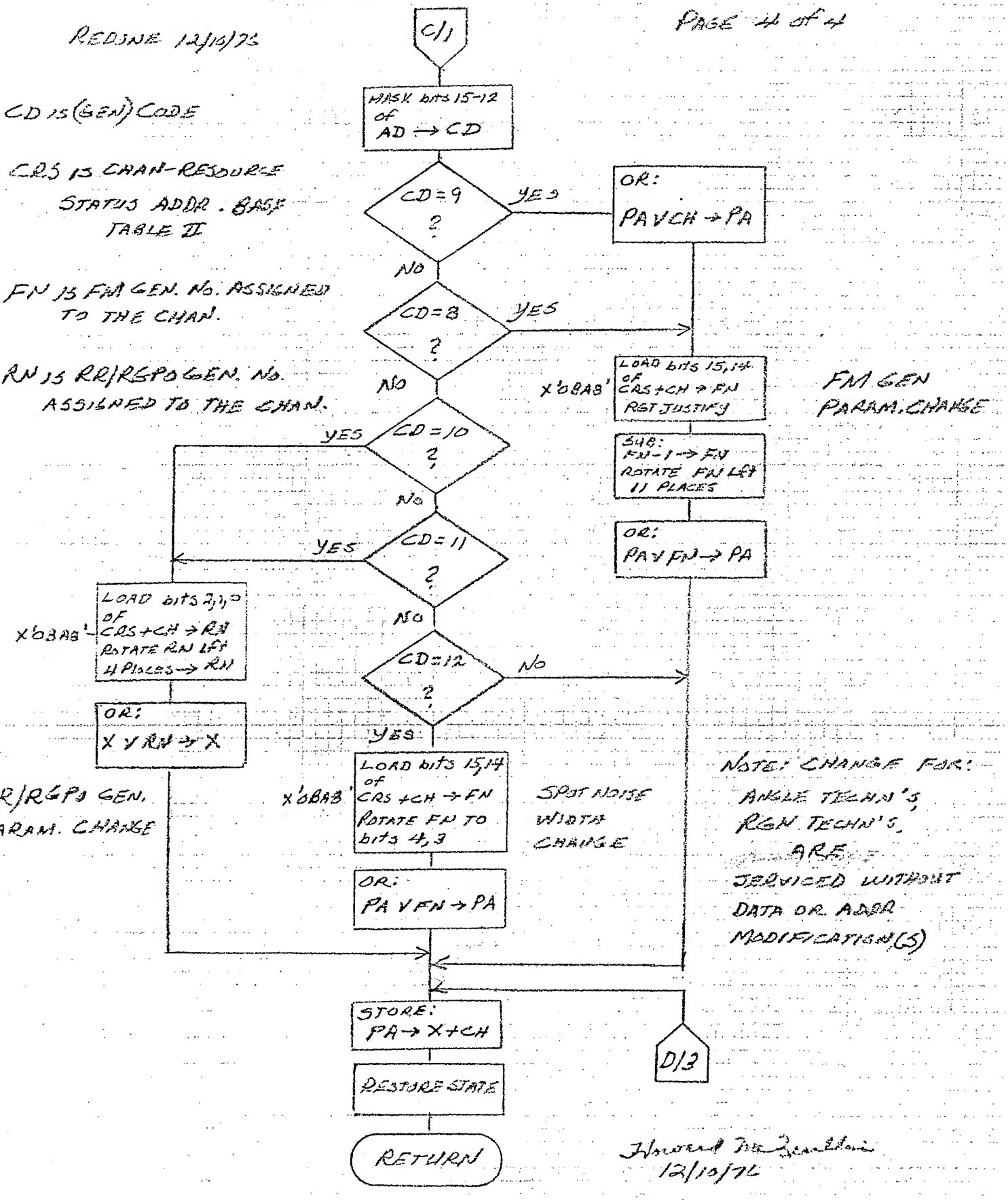
REDINE 12/16/71

CD IS (GEN) CODE

CRS IS CHAN-RESOURCE STATUS ADDR. BASE TABLE II

FN IS FM GEN. No. ASSIGNED TO THE CHAN.

RN IS RR/RGPS GEN. No. ASSIGNED TO THE CHAN.



Warren McClendon
12/10/71

Program memory. This module alternatively dismisses a particular Channel-Technique assignment. See notes of Figure 8 for codes. The routine for channel-technique dismissal also performs the resource management update of RAN-RAP/RGPO generator allocations.

3.2.7 SC Program Control (SCPC) Module

This module is a growth module to allow great flexibility to enable the TG RP-16 to execute instructions sent by the SC. The hardware is designed to accomodate this, but currently the SC External Control via hardware address is sufficient. See Figure 10 of 53959-HM-0410.

3.2.8 Channel-VCO Frequency Set-on (CVFSO) Module

CVFSO shall be the interrupt routines of Figure 9. This routine is requested every 0.1 second by each channel-technique assigned. It currently is a linear integration of error correction. Growth software could provide other correction to include even a transfer table for VCO tuning command to frequency output. The routine calls subroutine Convert and Load Tuning (CLT) to select VCO subband and tuning, within subband.

3.2.9 Auxiliary Bus Frequency (ABFR) Module

ABFR is the interrupt routine of Figure 10. This routine services frequency assignment updates for response-assigned channels, whose assignment includes Auxiliary bus update enable. The module uses the Frequency Update (FUP) subroutine which exits directly to LOOP.

3.2.10 RAN-RAP Cover (RRC) Module

RRC is the interrupt module of Figure 11. As noted thereon, this function is performed for each of the four RAN-RAP/RGPO generators. List I of paragraph 3.3 gives the priority level and least significant octal addresses for each generator service module. This module uses RAN-RAP A version (RRA) subroutine and generates a single element RAN-RAP. Internal

FIG. 9 CHANNEL-VCO FREQUENCY SET-ON

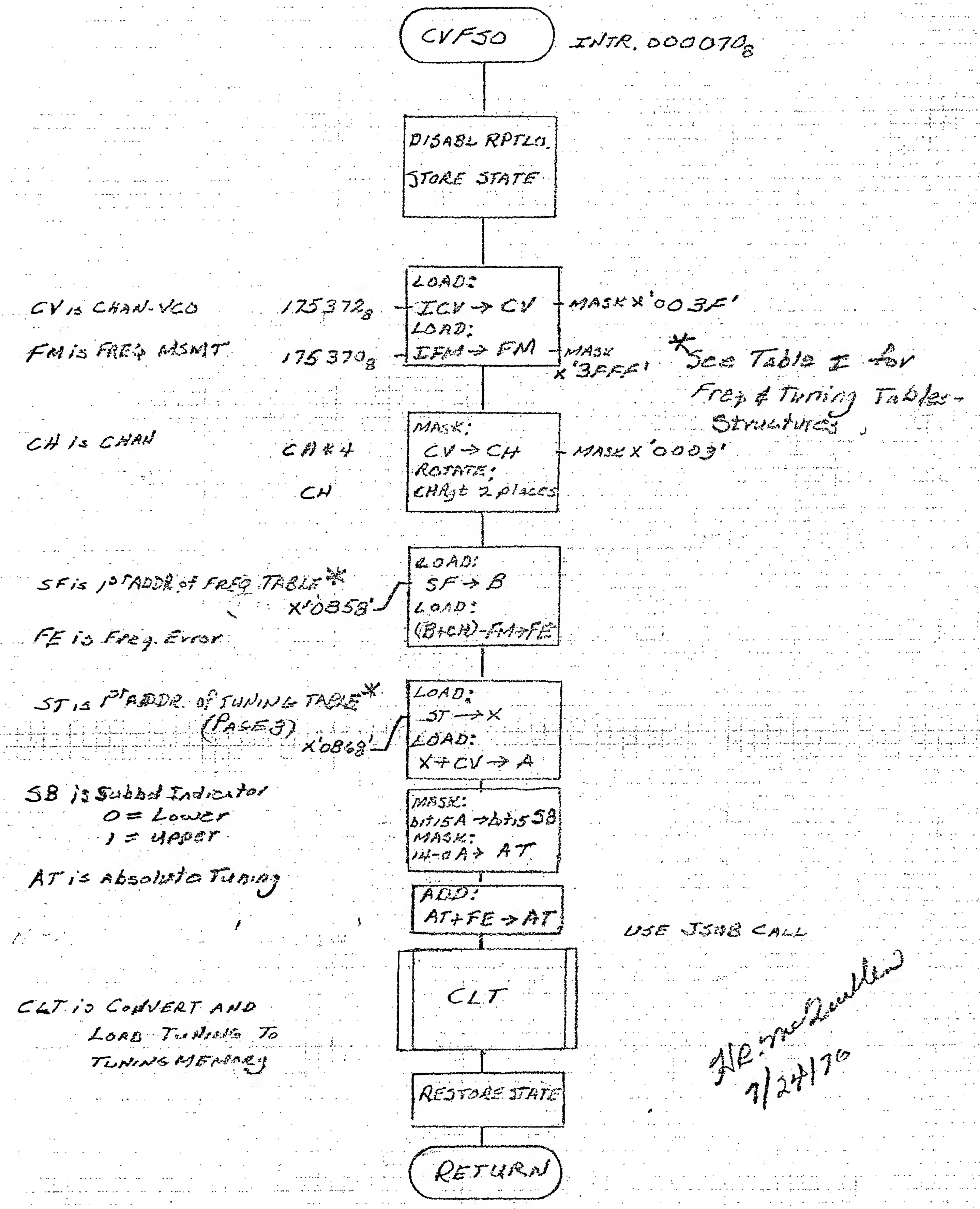
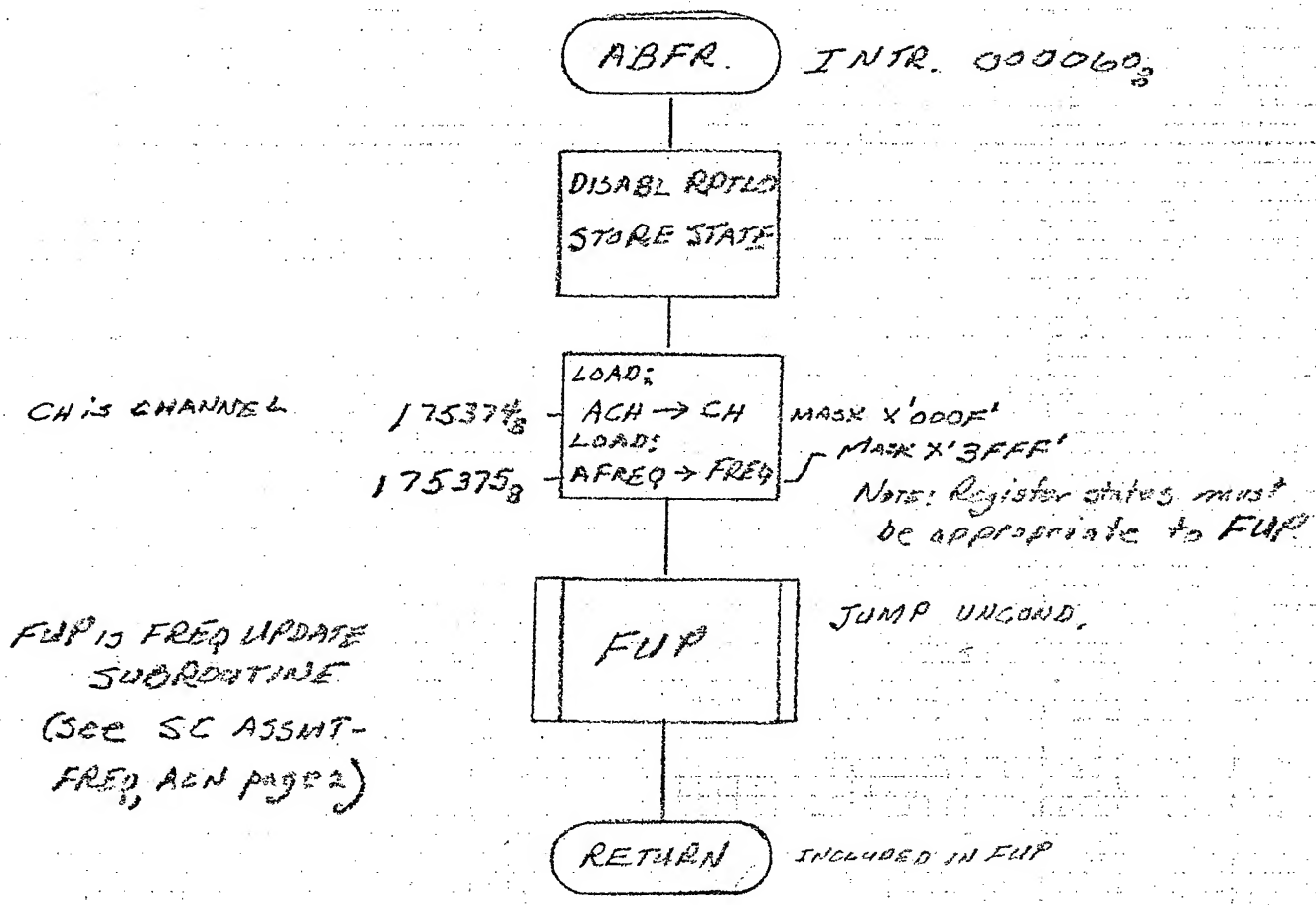


FIG. 10 AUX BUS FREQUENCY



F. McGuckin
7/21/76

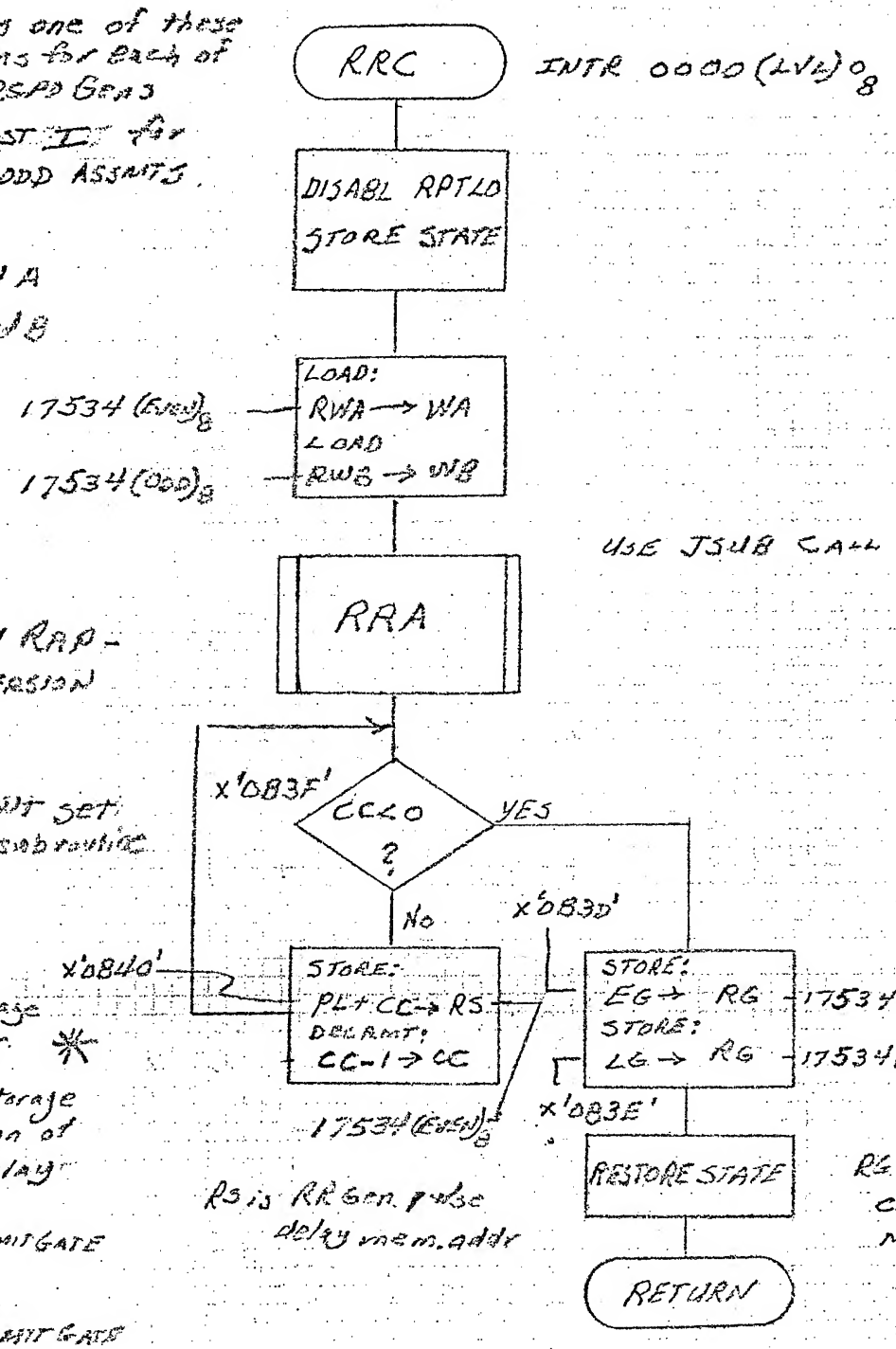
FIG. 11. RAN RAP COVER

NOTES: 1. There is one of these programs for each of 4 RR/RSPD Gens

2. See LIST II for LVL, EVEN, ODD ASSMTS.

WA is Word A

WB is Word B



* See TABLE III

A.R. McQuillen
7/29/76

pulse delay storage shall be as in Table III.

3.2.11 RAN-RAP Cover and Early (RRCE) Module

RRCE is the interrupt module of Figure 12. The description of paragraph 3.2.10 is generally the same except these routines generate a two-element RAN-RAP.

3.2.12 RAN-RAP Cover and Late (RRCL) Module

RRCL is the interrupt module of Figure 13. This is another two-element RAN-RAP similar to paragraph 3.2.11.

3.2.13 RAN-RAP Cover, Early and Late (RRCEL) Module

RRCEL is the interrupt module of Figure 14. This is a three-element RAN-RAP built up from the single element of paragraph 3.2.10. Note that growth software can have many variations in delay pulse configurations for this RRCEL as well as for RRC, RRCE, and RRCL.

3.2.14 Range Gate Pull Off (RGPO) Module

RGPO is the interrupt module of Figure 15. As noted thereon this function shall be performed for each of four RR/RGPO generators. List I gives the priority levels and addresses.

3.2.15 Frequency Update (FUP) Subroutine

FUP is the subroutine of Figure 16. As noted thereon frequency assignment modules SCAFA and ABFR shall use the subroutine. Internal tables used are those of Table I. Essentially this subroutine shall update the tuning of each of four VCO's by the same amount the channels assigned frequency is changed. Growth software can have a more complex tuning update if tests with MAAS equipment indicate a need. FUP uses the subroutine Convert and Load Tuning (CLT).

FIG. 12 RAN RAP COVER AND EARLY

NOTES: 1. There is one of these programs for each of 4 RR/RAPD Gens

2. See TABLE II for LVL, EVEN, ODD ASSMTS

WA is word A

WB is word B

RRA is Ran Rap A version

CC is Cell Count, Set by RRA

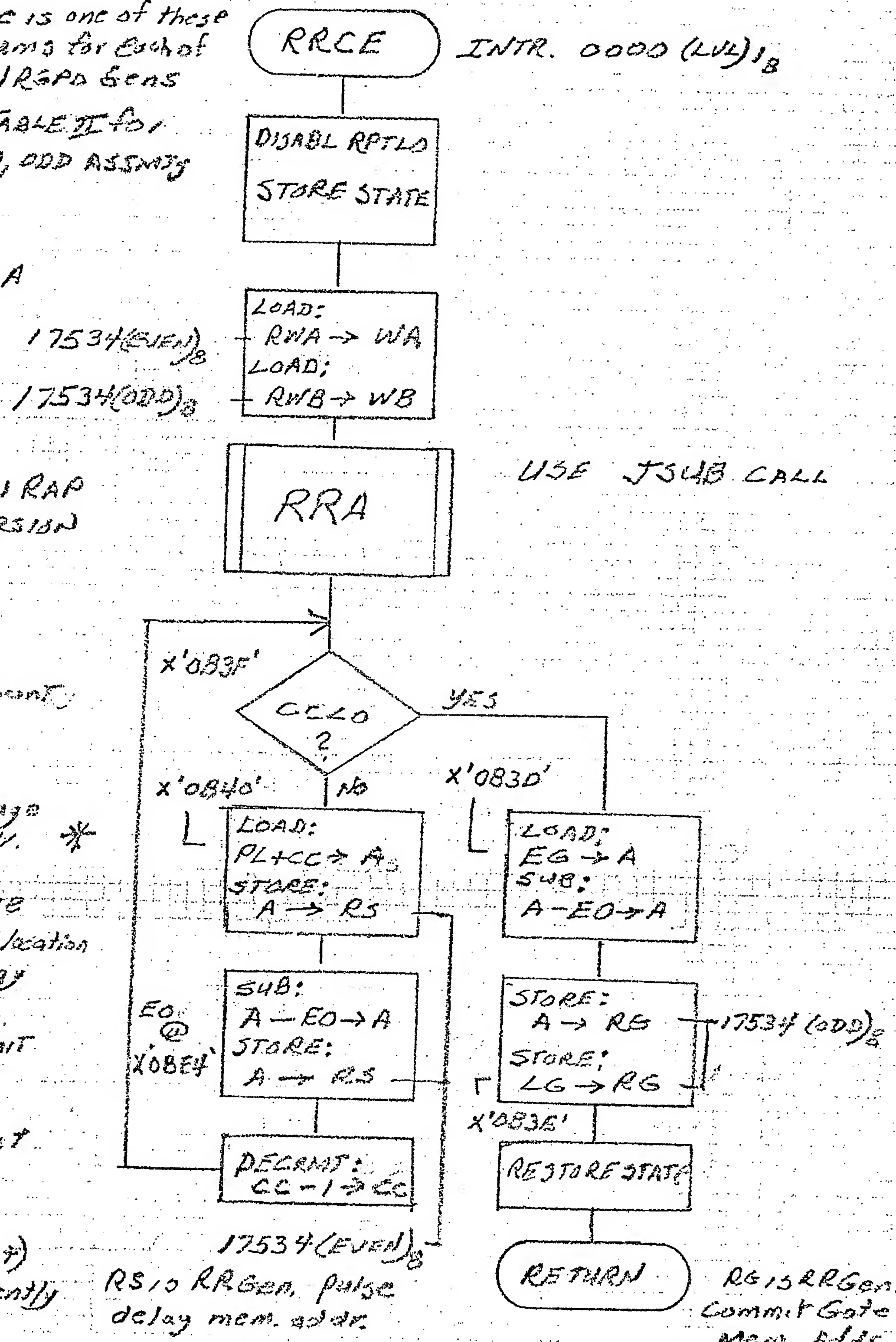
PL is pulse storage Start addr. *

CC is also relative storage cell location of pulse delay

EG is Early Commit Gate delay

LG is Late Commit Gate delay

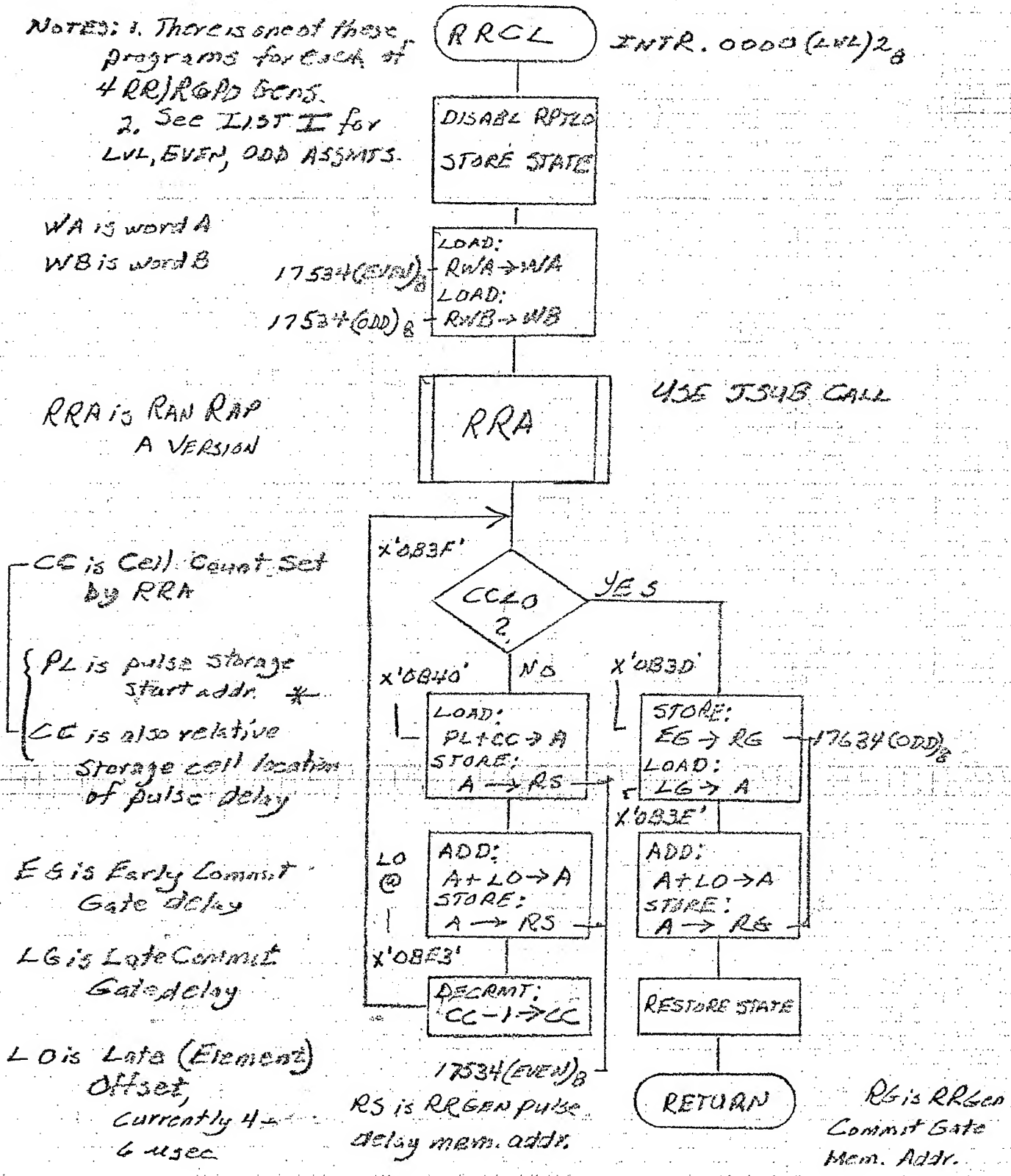
EO is Early (Element) Offset, currently 4 μsec



* See TABLE III

H.R. [signature] 7/30/76

Fig. 13 RAN RAP Cover and Late



* see TABLE III

N R McQuillen
7/30/73

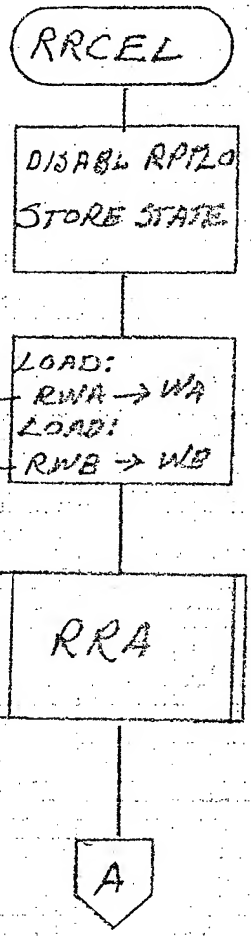
FIG. 14 RAN RAP - COVER, EARLY AND LATE

Page 1 of 2

NOTES; 1. There is one of these programs for each of 4 RB/RSPs GENS.
2. See LIST I for LVL, EVEN, ODD ASSMTS

WA is Word A

WB is Word B



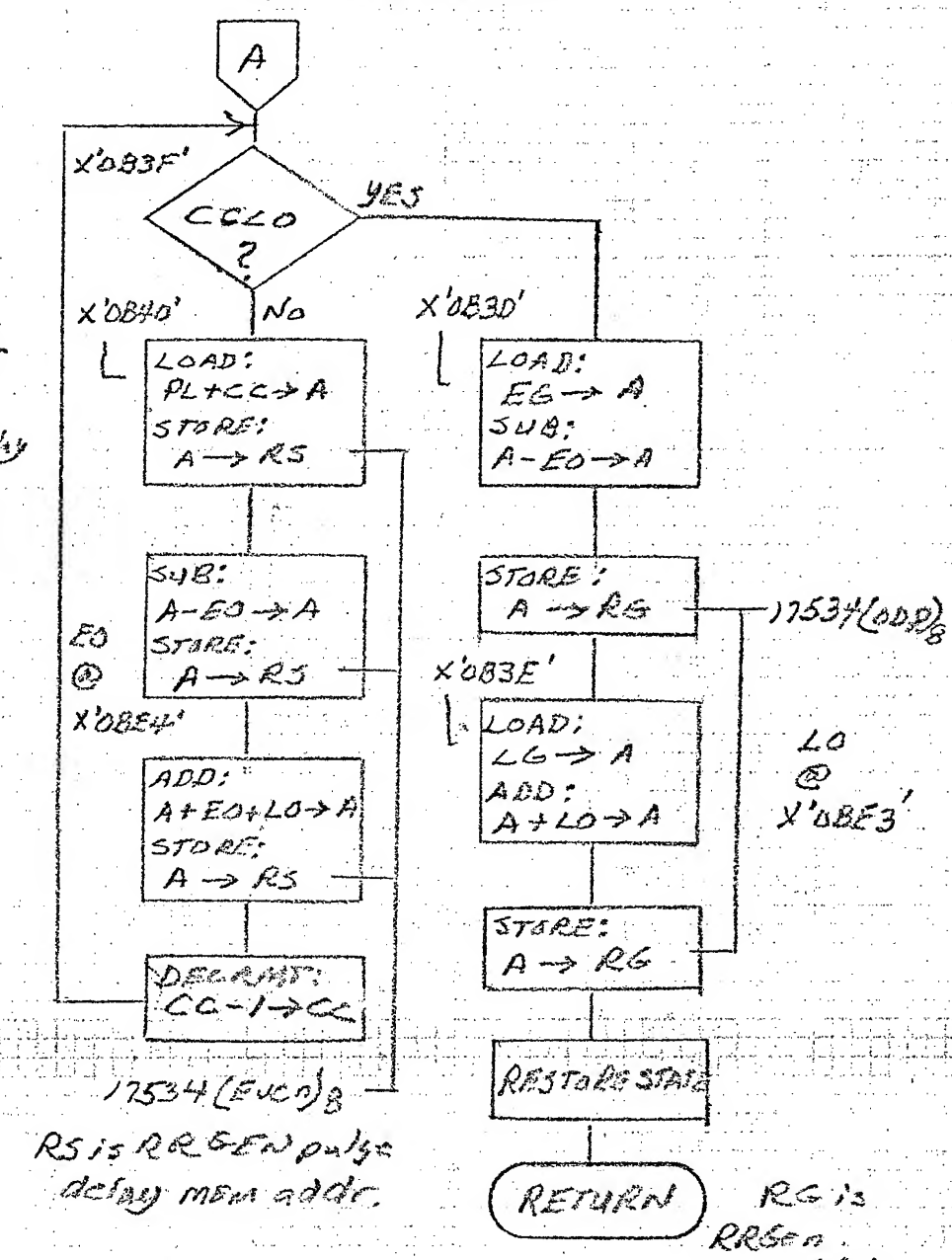
RRA is RAN-RAP A VERSION

17534(EVN)$_8$

17534(ODD)$_8$

A.R. McFadden
7/30/76

FIG 14 RAN RAP - COVER, EARLY AND LATE (CONT'D) PAGE 2 of 2



CC is Cell Count set by RRA

PL is pulse storage start addr *

CC is relative storage cell location of pulse delay

EG is Early Commit Gate delay

LG is Late Commit Gate delay

EO is Early (Element) Offset, currently 4 usec.

LO is Late (Element) Offset, currently 4 usec

RS is RRSEN pulse delay mem addr.

RG is RRSen Commit Gate mem addr.

* See TABLE III

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7/30/76

FIG 15 RANGE GATE PULL OFF

Page 1 of 2

NOTES: 1. There is one of these programs for each of 4 RR/REPRO GEN's.

2. See LIST I for LVL, EVEN, ODD ASSMTS

WB is WORD B

WA is WORD A

PW is Pulse Width

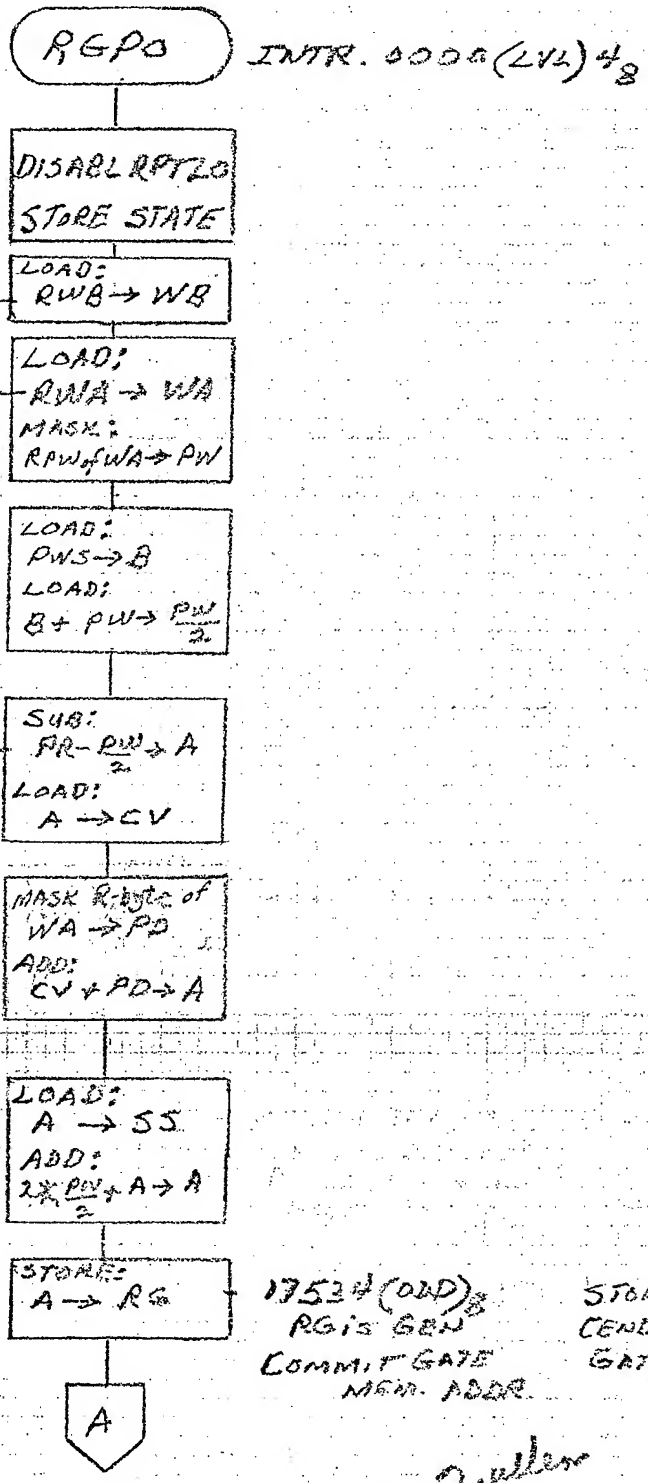
PWS is Start of pulse width conversion table. X'0BE5'

PR is pretrigger, currently 25.6 usec. LSB = 62.5 nanosec. X'0BE1'

CV is Cover PR + Delay

PD is Pull-off Delay

SS is SCRATCH-PAD delay STROBE



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7/26/76

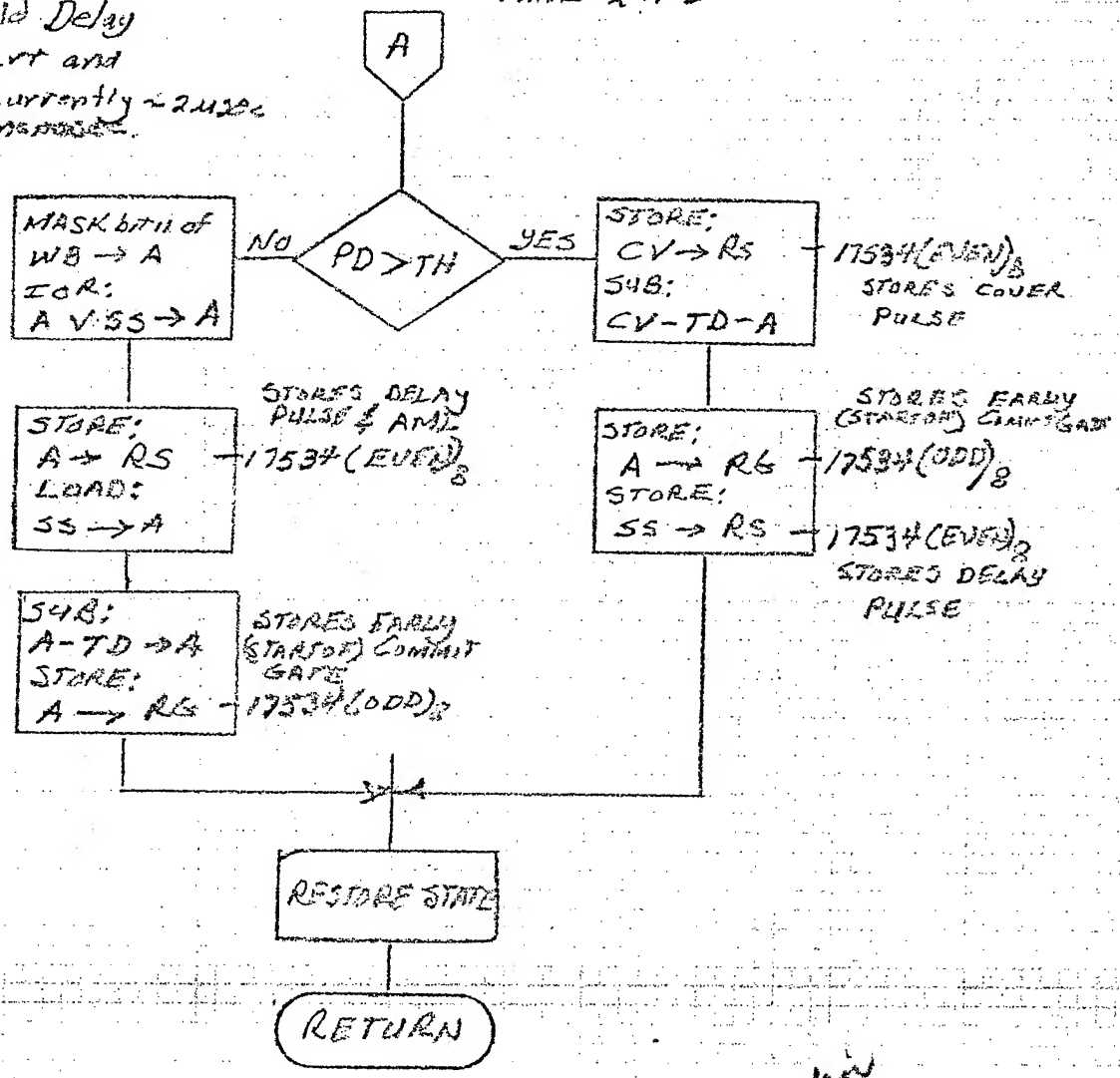
FIG. 15 RANGE GATE PULL-OFF (CONT'D)

PAGE 2 of 2

TH is Threshold Delay for Cover Start and AMI check, currently ~2 μsec. LSB = 62.5 nanosec.

TD is TUNING DELAY, currently ≥ 10 μsec. LSB = 62.5 nanosec.

bit 11 of WB is AMI bit
1 → AMI
0 → $\overline{AMI}$



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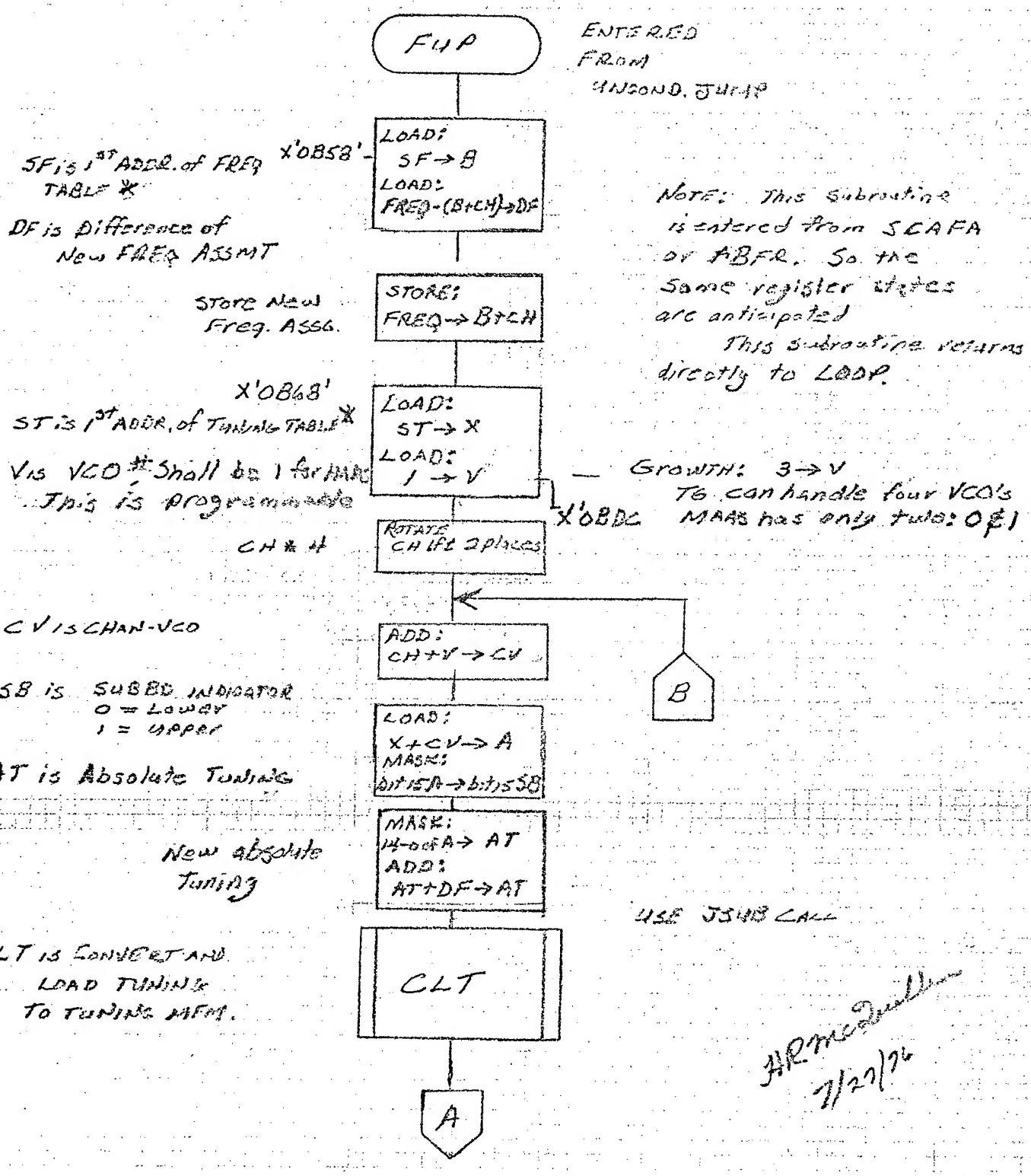
7/26/74

FIG. 16 FREQUENCY UPDATE SUBROUTINE Page 1 of 2

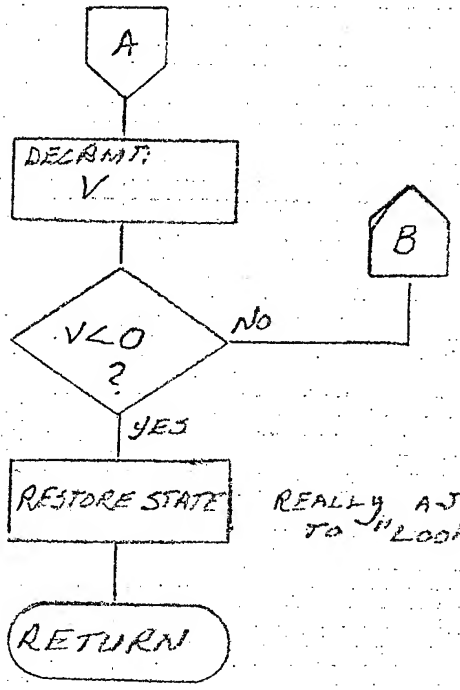


A.R. Meador 11/27/74

*See TABLE I for Freq & Tuning Tables - Structures.

Fig. 16 FREQ UPDATE SUBR. (CONT'D)
FUO

Age 2 of 2



J R McCandless
1/27/76

3.2.16 Convert and Load Tuning (CLT) Subroutine

CLT is the subroutine of Figure 17. This subroutine shall convert the calculated absolute tuning frequency to tuning frequency by subband designation and relative subband tuning command. This routine assumes an upper subband VCO in the MAAS transmitter. It includes hysteresis for overlap of subbands, and assumes subband tuning is proportional above a lower value for each subband. The overlap and the lower values of each subband are programmable.

3.2.17 RAN-RAP A Version (RRA) Subroutine

RRA is the subroutine of Figure 18. This subroutine sets up the basic element pulse delay patterns for all RAN-RAP programs. It also sets up the basic commit gate start and end.

3.3 STORAGE AND PROCESSING ALLOCATION

The Technique Generator RP-16 Controller memory allocations are given in Figure 15 of reference 53959-HM-0410. Of the 4K-word memory, the upper 1K is currently allocated to T.G. Techniques Program memory. Within the remaining 3K, the software instructions and data objects of this CPDS are to fit. All other addresses are given in the cited reference and listed herein where needed.

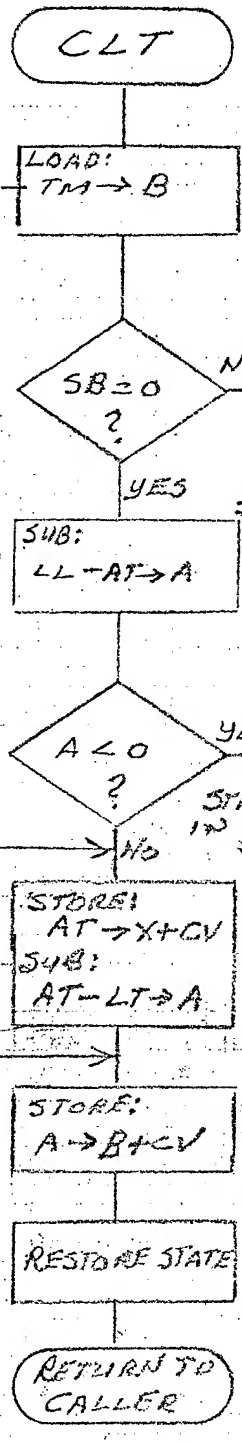
Tables I through III are the important internal data-object tables for the T.G. Controller Program. Use of these tables is given in the appropriate functional description of paragraph 3.1. List I gives the RR/RGPO Generators priority and address assignments. List II summarizes important program data objects. List III allocates total RP-16 addresse space, including programs and data.

3.4 COMPUTER PROGRAM FUNCTIONAL FLOW

Program flow is described in paragraph 3.1 and Figure 1, and 2. Interrupt levels and assignments are given therein.

FIG. 17 CONVERT AND LOAD TUNING (TO TUNING MEMORY) SUBROUTINE

Page 1 of 2



SUBROUTINE IS ENTERED FROM CALLERS CVFSO OR FUP - Needs Correct Register States

TM is start of TUNING MEMORY 175200$_8$

SB is SUBBD INDICATOR
0 = Lower
1 = Upper

UPPER SUBBD TEST

LOWER SUBBD TEST

LL is LIMIT OF LOWER SUBBD, currently ≅ 12 GHz
LSB = 1.25 MHz
AT is Absolute Tuning from Caller X'0BDE'

GO TO UPPER SUBBD

STAY IN LOWER SUBBD

LT is Lower (SUBBD) Threshold currently ≅ 8GHz
LSB = 1.25 MHz
See Callers For X & CV
X is ST X'0B68'

LT @ X'0BDD'

NOTE: AT has SB=0.

LEAVES SUBBD Flag = 0

STORES Relative tuning & SUBBD Flag. Generic Exit

NOTE: THIS SUBROUTINE CAN BE EXPANDED TO INCLUDE VCO TUNING CURVES IF LATER VCO TESTS SO INDICATE

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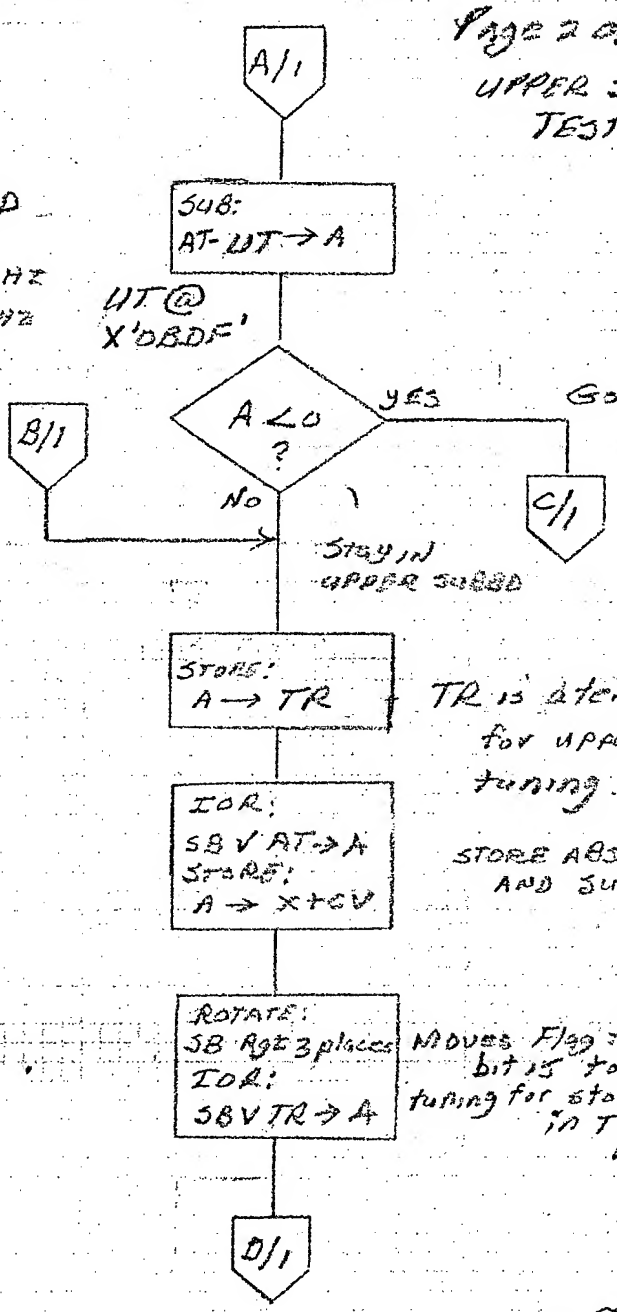
FIG 17 CONVERT AND LOAD TUNING SUBROUTINE (CONT'D)

Page 2 of 2

UPPER SUBBD TEST



UT IS UPPER SUBBD THREE

Should be ≈ 11.8 GHz

LSB = 1.25 MHz

Go to lower SUBBD

X is from Caller,

X = ST

TR is a temporary register for upper subB relative tuning.

STORE ABSOLUTE TUNING AND SUBBD FLAG.

MOVES Flag from bit 15 to bit 12, and includes rel. tuning for storage in TUNING MEMORY.

JLR mr Dwiller

7/27/76

FIG. 18 RAN RAP A VERSION

SUB ROUTINE

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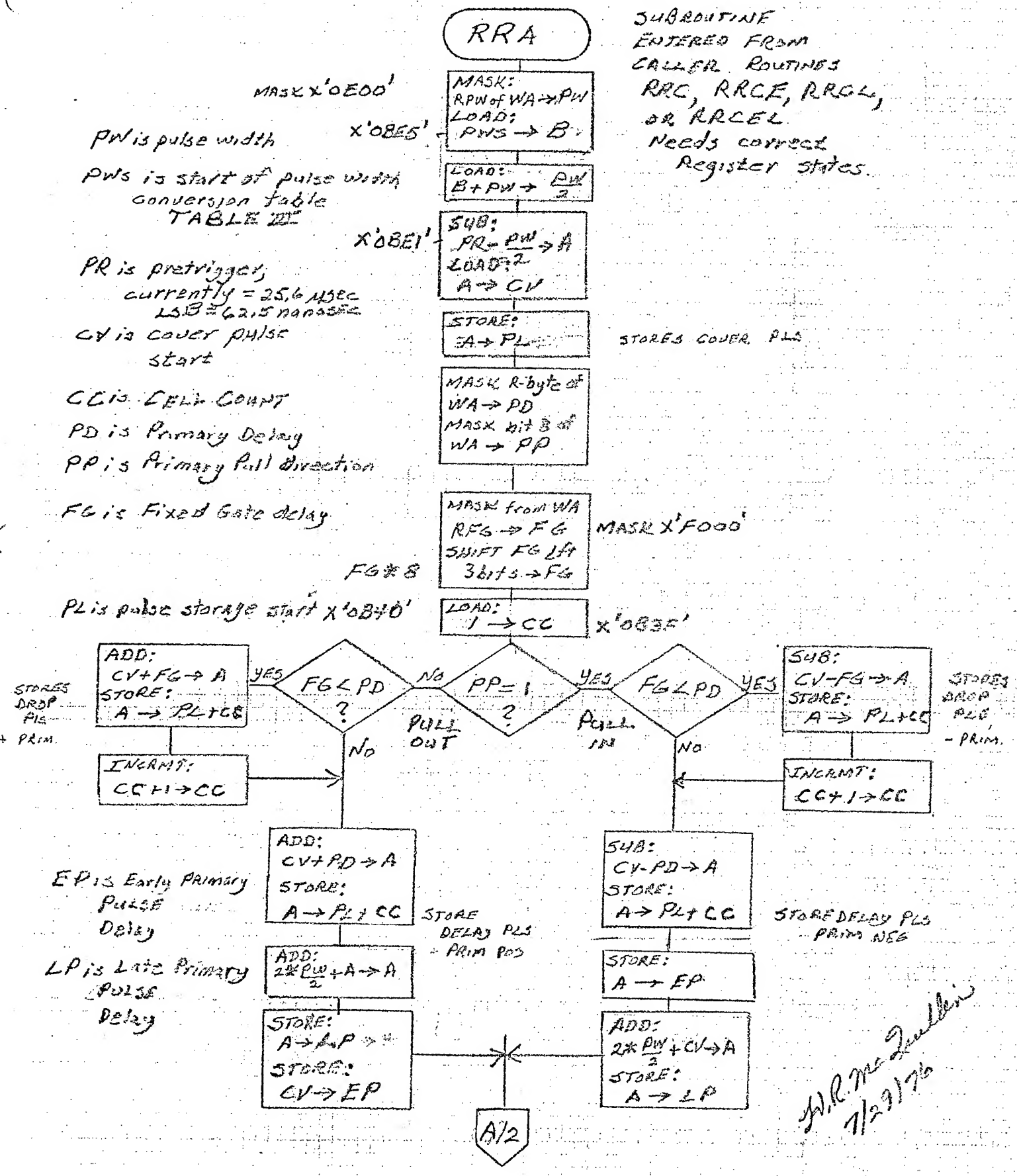
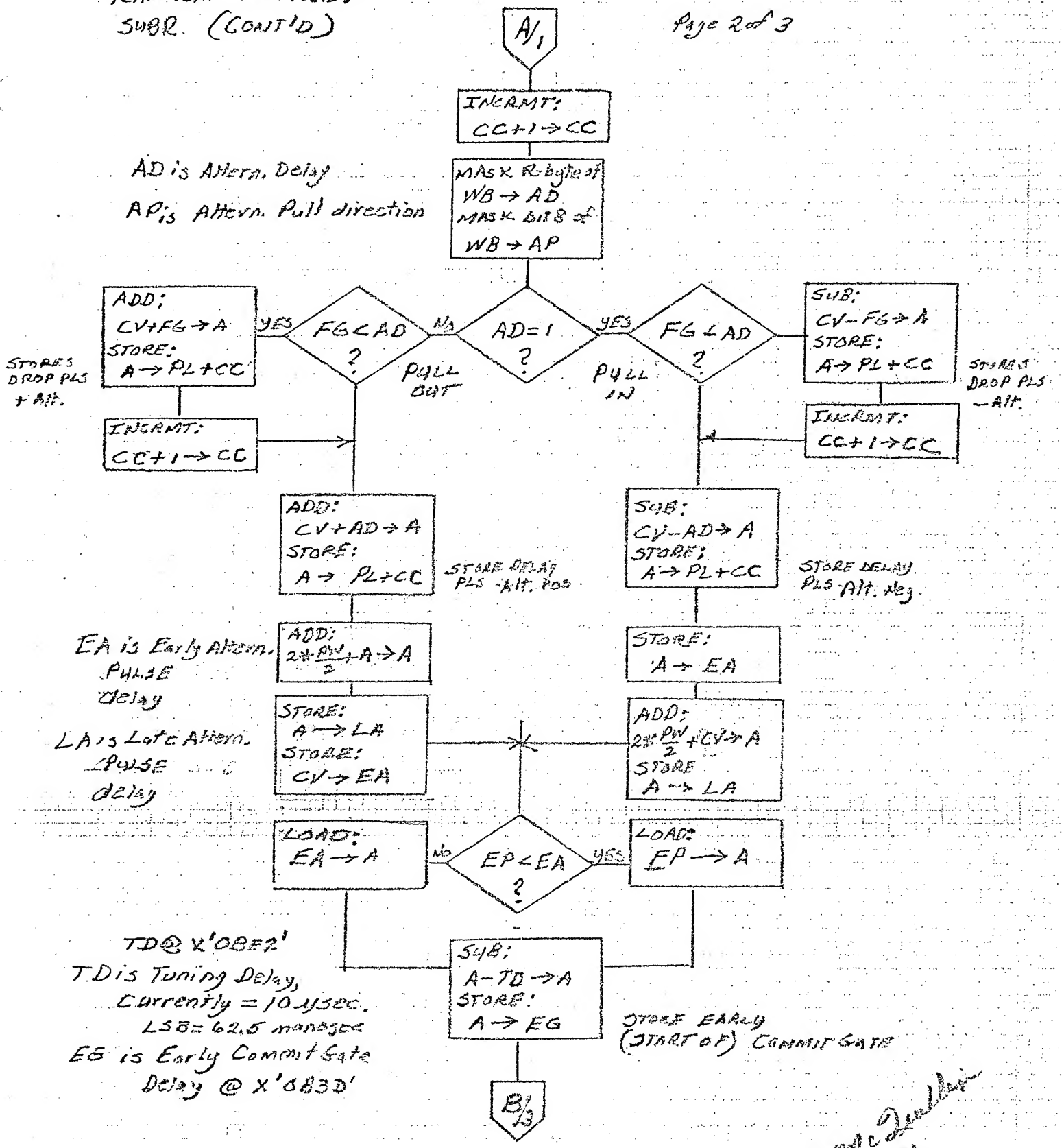


W.R. McQuilkin 1/21/76

FIG. 18
RAN-RAP AVERSION
SUBR. (CONT'D)

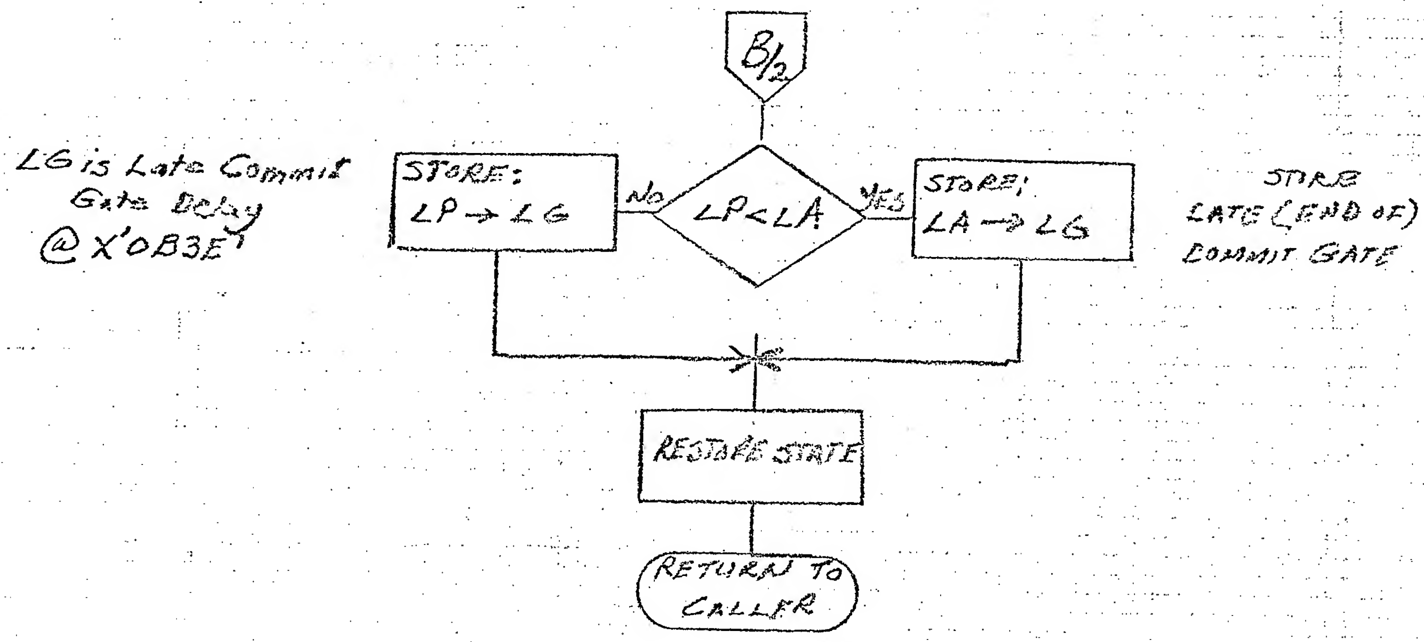
Page 2 of 3



HR McAuliffe
7/23/76

FIG. 1B
RAN-RAP A VERSION
548R (CONT'D)

Page 3 of 3



H.R. McMullen
7/29/76

TABLE I FREQUENCY AND TUNING LOCAL DATA STRUCTURES

SF is FREQ ADDR. BASE

ADDRESS CH	DATA LSB = 1.25 MHz
SF + 0_H	FREQ (0_H) ... 14 bits
• • •	• • •
SF + F_H	FREQ (F_H)

ASSIGNED FREQUENCY TABLE

ST is TUNING Addr. BASE

ADDRESS CV	DATA is AT = Absolute TUNING LSB = 1.25 MHz. AND
ST + $0_H 0_B$	TUN ($0_H 0_B$)
ST + $0_H 1_B$	TUN ($0_H 1_B$)
ST + $0_H 2_B$	TUN ($0_H 2_B$)
ST + $0_H 3_B$	TUN ($0_H 3_B$)
• • •	• • •
ST + $F_H 0_B$	TUN ($F_H 0_B$)
ST + $F_H 1_B$	TUN ($F_H 1_B$)
ST + $F_H 2_B$	TUN ($F_H 2_B$)
ST + $F_H 3_B$	TUN ($F_H 3_B$)

Bit 15: 0 → SUBBD 1 - LOWER; 1 → SUBBD 2 - UPPER

TUNING TABLE

ALSO SEE LIST III

NOTE: These are used in Freq. UPDATE (FUP) SUBROUTINE, AND CHANNEL-VCO FREQ DETAIL (CVFRQ) MODULE.

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7/30/76

TABLE II CHANNEL-RESOURCE, AND RESOURCES LOCAL DATA STRUCTURES

CRS is CHAN-RESOURCE STATUS ADDR. BASE

USED BY INITIALIZATION (INLZ) MODULE, SC TECH ASSMT (SCTA) MODULE AND SC TECH-CH PARM. CHG OR DISMISS MODULE (SCTCC).

ADDRESS	CH	DATA-bits 15,14	13 - 3	2-0
CRS	+ 0_H	FN	ZERO	RN
.	. .	.	.	.
CRS	+ F_H	FN	ZERO	RN

CHANNEL-RESOURCE TABLE

FN - OCTAL
0 - NONE
1 - GEN #1
2 - GEN #2

RN - OCTAL
0 - NONE
1 - GEN 1
2 - GEN 2
3 - GEN 3
4 - GEN 4

SRS is RR/RGPO GEN STATUS ADDR. START

USED BY INITIALIZATION (INLZ) MODULE

ADDRESS	RN RR/RGPO GEN #	DATA - HEX
SRS	+ 1_8	0005_H
.	. .	. . .
SRS	+ 4_8	0005_H

RR/RGPO GENERATOR PRE-OPERATION STATUS TABLE

HEX 5_H	MEANING
0	AVAILABLE
1	NOT AVAILABLE

SRA is RR/RGPO GEN. ALLOCATION ADDR.

USED BY INITIALIZATION (INLZ) MOD, SC TECH ASSMT. (SCTA) MODULE, AND SC TECH-CH DISMISS (SCTCC) MODULE

ADDRESS	RN RR/RGPO GEN #	DATA HEX
SRA	+ 1_8	$000A_H$
.	. .	. . .
SRA	+ 4_8	$000A_H$

RR/RGPO GENERATOR ALLOCATION (OPERATION) TABLE

HEX A_H	MEANING
0	NOT ALLOCATED
1	ALLOCATED

ALSO SEE LIST III

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7/30/76
REVISED 11/29/76

TABLE II.A RESOURCES LOCAL DATA STRUCTURE CONTINUED

	ADDRESS			DATA HEX
		FM GEN #	FM GEN #	
SFS IS FM GEN STATUS ADDR START	SFS	+	1	0 0 0 S_H
	SFS	+	2	0 0 0 S_H

HEX	
S_H	MEANS
0	AVAILABLE
1	NOT AVAILABLE

USED BY INLE MIR

FM GENERATOR PRE-OPERATION STATUS TABLE

	ADDRESS			DATA HEX
		FM GEN #	FM GEN #	
SFA IS FMGEN ALLOCATION ADDR	SFA	+	1	0 0 0 A_H
	SFA	+	2	0 0 0 A_H

HEX	
A_H	MEANS
0	AVAILABLE
1	NOT AVAILABLE

USED BY INLE, SCTA, SCTLE MODS

FM GENERATOR ALLOCATION (OPERATION) TABLE

Howard McDaniel
11/29/76

TABLE III RAN-RAP PULSE DELAY STORAGE AND PULSE WIDTH CONVERSION TABLE

PL is pulse storage start
CC is cell count
Used by All RAN-RAP Modules And SUB ROUTINE.

ADDRESS CC CELL COUNT	DATA bits 7-0 USED LSB = 62.5 NANOSEC.
PL + 0	PULSE DELAY (1)
. . .	. . .
PL + 5	PULSE DELAY (4)

NOTE: ALLOW FOR 2 1/2 LOCATIONS

RAN-RAP PULSE DELAY TABLE

PWS is Pulse Width Conversion

ADDRESS PW PULSE WIDTH CODE	DATA - PW/2 bits 5-0 LSB = 62.5 nanosec
PWS + 1_8	1.5 usec = 30_8
+ 3_8	1.0 usec = 20_8
+ 5_8	0.5 usec = 10_8
+ 6_8	0.25 usec = 4_8

PULSE WIDTH CONVERSION TABLE

ALSO SEE LIST III

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1/30/74

LIST I RR/RGPO GENERATES- PRIORITY LEVEL, AND ADDRESS LSB ASSIGNMENTS

GEN#	(PRIORITY) LVL$_8$	WRITE ADDRESS 3 LSBs EVEN$_8$*	ODD$_8$ #
1	5	0	1
2	4	2	3
3	3	4	5
4	2	6	7

HIGHER NUMBER ~ HIGHER PRIORITY

* PULSE STROBE DELAY MEMORY

COMMIT GATE DELAY MEMORY

J.R. McQuillan
1/30/76

LIST II IMPORTANT DATA-OBJECTS AND USERS

DATA ITEM		USING MODULE(S) OR SUBROUTINE(S)
REF.	DESCRIPTION	
CT	Count - No. LOOP entries after INL2	INL2, LOOP
CRS	Channel Resource Table Start	INL2, SCTA, SCTCC
SRS	Start of RR/RGPO Status Table - Pre-Run Programmable	INL2
SRA	Start of RR/RGPO Allocation Table - During Run	INL2, SCTA, SCTCC
PS	(Technique) Program Start - 006000_8 Pre-Run Prgrmbl.	SCTA, SCTCC
SF	Start of Frequency (Assignment) Table	CVFSO, FUP
ST	Start of Tuning (Absolute) Table	CVFSO, FUP
PL	Pulse Storage Start	RRC, RRA, RRCE RRCL, RRCEL
EG	Early (Commit) Gate - start	RRC, RRA, RRCE RRCL,
LG	Late (Commit) Gate - end	RRC, RRA, RRCE RRCL, RRCEL,
TD	Tuning Delay Pre-Run Programmable	RRA
PR	Pretrigger Delay Pre-Run Programmable	RRA

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7/30/76

LIST II (CONT'D) IMPORTANT DATA-OBJECTS AND USERS

DATA ITEM		USING MODULE(S) OR SUBROUTINE
REF.	DESCRIPTION	
EO	Early (Element) Offset Pre-Run Programmable	RRCE, RRCEL
LO	Late (Element) Offset Pre-Run Programmable	RRCL, RRCEL
PWS	Pulse Width Conversion Start Table Pre-Run Programmable Table Fixed	RRA
CH	Channel VARIABLE 0 thru 15	INLZ, SCAFA, SCTCC, CVFSO, ABER
RN	RR/RGPO. GEN. Abs. VARIABLE 1 thru 4	INLZ, SCTA, SCTCC
AN	ANGLE CELL NO. VARIABLE 0 thru 31 Growth thru 63	SCAFA
TN#8	Technique No. VAR. 0000_8 through 1770_8 with LSB always 0_8	SCTA, SCTCC
CC	Cell Count-RAN-RAP Delay Pulse No. VARIABLE	RRC, RRA, RRCE, RRCL, RRCEL
TH	Threshold Delay for Cover insert FAME Pre-run Programmable	RGPO
LL	Lower Subband Limit Tune (Highest) Pre-run Programmable	CLT
LT	Lower Subband Threshold Tune Freq. Pre-run Programmable	CLT
UT	Upper Subband Thres. Tune (Lowend) Pre-run Programmable	CLT

A.R. Mc Quillen
1/30/76

3.5 PROGRAMMING GUIDELINES

Object program shall be machine code suitable for loading from the System Controller (SC) via the Daisy Chain (DC) bus. During development object program shall be available on paper tape for loading via a TTY terminal directly into the T.G. The latter includes an Asynchronous Line Control Module (ALCM) for TTY interface and a Hardware Loader program to accept inputs. Word formats and addresses are given in Figures 15, 16 and 17 of reference 53959-HM-0410.

Source programming can be in assembly language. The source program can be converted to object program using either the RP-16 Assembler, reference Equipment Division II, or the ESD Nova Cross-Assembler for the RP-16. RP-16 instructions and functions are described in reference Equipment Division I.

LIST III TGU RP-16 ADDRESS SPACE PAGE 1 OF 4

LOCATION HEX	DATA	DATA TYPE
0000	VECTOR ADDR. "INLZ" = X'0050'	(START OF 4K MEM.) DEFINED 1_{10}
0001 ... 006F	INTERRUPT VECTOR ADDR's CURRENT & GROWTH SEE TGU HARDWARE SPEC	DEFINED DURING CODING & ASSY. 111_{10}
INLZ = 0070	T.G. PROG INSTR's: START INLZ & PROG. DATA NOT ELSEWHERE	INSTR & DATA
...		912_{10}
03FF	ESTIMATED LIMIT OF PROG INSTR/DATA	
0400	GROWTH ↓	1853_{10}
	↑ STACK	
STACKI-1 = 083C	TOP OF STACK USED	VAR.

TOTAL = 2877

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LIST III TGU RP-16 ADDRESS SPACE (CONT'D) PAGE 2 of 4

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LOCATION HEX	DATA	DATA TYPE	
EG = 0B3D	EARLY GATE - RAN-RAP	VAR	1_{10}
LG = 0B3E	LATE GATE - RAN-RAP	VAR	1_{10}
CC = 0B3F	CELL COUNT - # RR PL'S	VAR	1_{10}
PL = 0B40 ... 0B57	PULSE STORAGE FOR RAN-RAP	VAR	24_{10}
SF = 0B58 ... 0B67	FREQ (ABSOLUTE) FOR CHANNEL ASSIGNMENTS - TABLE I	VAR.	16_{10}
ST = 0B68 ... 0BA7	TUNING (ABSOLUTE) FOR CHAN-VCO ASSGNMTS - TABLE I	VAR.	64_{10}
CRS = 0BA8 ... 0BB7	CHANNEL-RESOURCE TABLE - TABLE II	VAR.	16_{10}
SFA = 0BB8 / 0BB9 / 0BBA	BASE / GEN #1 / GEN #2 } FM GEN. CURRENT OPERATION ALLOCATION TABLE II A	VAR	3_{10}
SFS = 0BBB / 0BBC / 0BBD	BASE / GEN #1 / GEN #2 } FM GEN. PRE-OPER STATUS TABLE II A	PRE-PROG'D	3_{10}
0BBE ... 0BDB	NOT USED - RESERVE		30_{10}
V = 0BDC	HIGHEST No. of VCO. For MAAS enter 1.*	PRE-PRGRMD	1_{10}
		TOTAL	160_{10}

* Note: TGU can handle 3, i.e. four VCO's
VCO's are numbered: 0, 1, ...

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7/8/76
REV 11/29/76

LIST III TGU RP-16 ADDRESS SPACE (CONT'D) PAGE 3 OF 4

LOCATION HEX	DATA	DATA TYPE	
LT = 0BDD	LOWER SUBBD THRES. TUNE	PRE-PRGMD (USE VALUES IN FLOW CHARTS)	
LL 0BDE	LOWER SUBBD HI LIMIT TUNE		
UT = 0BDF	UPPER SUBBD THRES TUNE		
TH = 0BE0	THR. DELAY FOR COVER, AMI RGPO		8,10
PR = 0BE1	RR/RGPO PRE-TRIG DELAY		
TD = 0BE2	RR/RGPO TUNING DELAY		
LO = 0BE3	RR LATE OFFSET		
EO = 0BE4	RR EARLY OFFSET		
PWS = 0BE5 ... 0BEC	PULSE WIDTH CONVERSION TABLE - RR/RGPO	PRE-PRGMD (USE TABLE III NOW)	8,10
SRA = 0BED	NOT USED — GROWTH		1,0
0BEE ... 0BF1	GEN #1 ... GEN #4 } RR/RGPO GEN. CURRENT OPERATION ALLOCATION TABLE II	VAR.	4,0
SRS = 0BF2	NOT USED - GROWTH		1,0
0BF3 ... 0BF6	GEN #1 ... GEN #4 } RR/RGPO GEN. PRE-OPER. STATUS TABLE II	PRE-PRGMD (PROG. ALL AVALBL NOW)	4,0
0BF7 ... 0BFF	SC-TG MESSAGE REG'S SEE TGU HARDWARE SPEC	VAR.	9,0

TOTAL 35,0

AR McQuillen
9/8/75

LIST III TGU RP-16 ADDRESS SPACE (CONT'D) PAGE 4 OF 4

	LOCATION HEX	DATA	DATA TYPE	
	0C00	TECHNIQUE PROGRAM	PRE-PRGMD	
	...	MEMORY	(TO BE SUPPLIED)	1023_{10}
4095_{10}	0FFF	SEE TGU HARDWARE SPEC FOR FORMAT	(END OF 4K MEM.)	
	1000			
	...	GROWTH PERIPH.		$59,904_{10}$
	E2FF			
$64,000_{10}$	FA00	TG INTERNAL PERIPHERALS	VAR.	
	...	SEE FLOW CHARTS AND		256
	FAFF	TGU HARDWARE SPEC.		
	FB00			
		GROWTH		256
	FBFF			
$64,512_{10}$	FC00	ALCM STATUS/CNTRL REG	VAR.	1,0
	FC01	ALCM DATA REG.	VAR	1,0
	FC02			
		GROWTH		765_{10}
	FEFE			
	FEFF	PIN DISABL REG.	VAR.	1,0
	FF00	FIRMWARE PROGRAM - PIN	FIXED	
	...	HARDWARE LOADER	INSTR.	254_{10}
$65,535_{10}$	FFFF			

TOTAL = $62,464_{10}$

H. B. McDowell
9/8/76

TABLE A. TGU SOFTWARE-TECHNIQUES PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 9	0C48	0021
XILM, RGN	9	1D82
	A	2140
	B	3000
	C	C004
	D	DB76
	E	F833
No. 13	0C68	0020
XICS-1, RGN	9	1CA4
	A	22A2
	B	3080
	C	C004
	D	D933
	E	F830
No. 31	0CF8	0020
XICS-2, RGN	9	1524
	A	2142
	B	30C1
	C	C003
	D	DF54
	E	F830

TABLE A. TSU SOFTWARE TECHNIQUES
PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 41	0D48	0020
XASWM-C, RGPO	9	1692
	A	2142
	B	3061
	C	A61C
	D	B347
	E	C005
	F	F830
No. 53	0DA8	0020
XASWM-C, RGN, FM	9	1A82
	A	2505
	B	3126
	C	84D4
	D	93C0
	E	C002
	F	D947
	0DB0	F830
No. 65	0E09	000C
XSSWM, RR-3	9	1208
	A	2000
	B	3086
	C	A31B
	D	B99C
	E	C004
	F	F830

TABLE A. TGU SOFTWARE-TECHNIQUES PROGRAM MEMORY DATA

PROGRAM	ADDRESS	DATA
No. 73	0E48	0020
XASWM-T, RR-3	9	1709
	A	2040
	B	3095
	C	A31B
	D	B99C
	E	C004
	F	F830
No. 91	0ED8	0020
RCW, ASWM-C	9	1480
	A	2281
	B	3147
	C	F520